Alignment Monitor

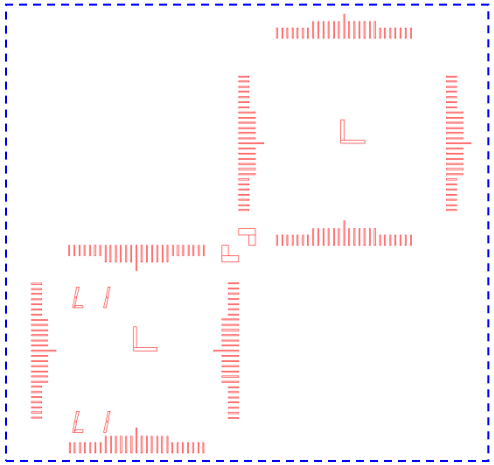
April 3, 2012

Process Flow

1. silicon piece coated with ZEP520
2. exposed global and chip marks
3. etched marks into silicon
4. strip resist
5. coat with ~340 nm ZEP520
6. align and expose vernier pattern 1, window 3B, with 3 different alignment types (4 chip marks, 1 chip mark and just global marks)
7. unload cassette, unload piece from cassette
8. reload piece, reload cassette
9. align and expose vernier pattern 2, window 3B, with 3 different alignment types
10. wrote 5um squares around chip marks
11. unload
12. simultaneous develop of step 5 and step 8
13. inspect in microscope

Pattern

alignment and
first exposure



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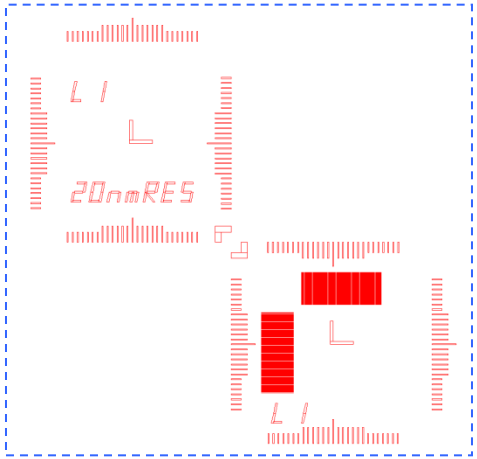
alignment and
second exposure



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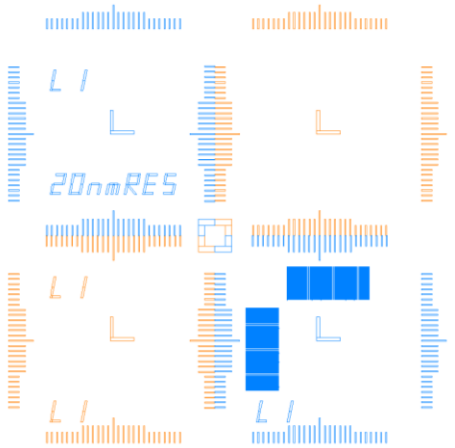
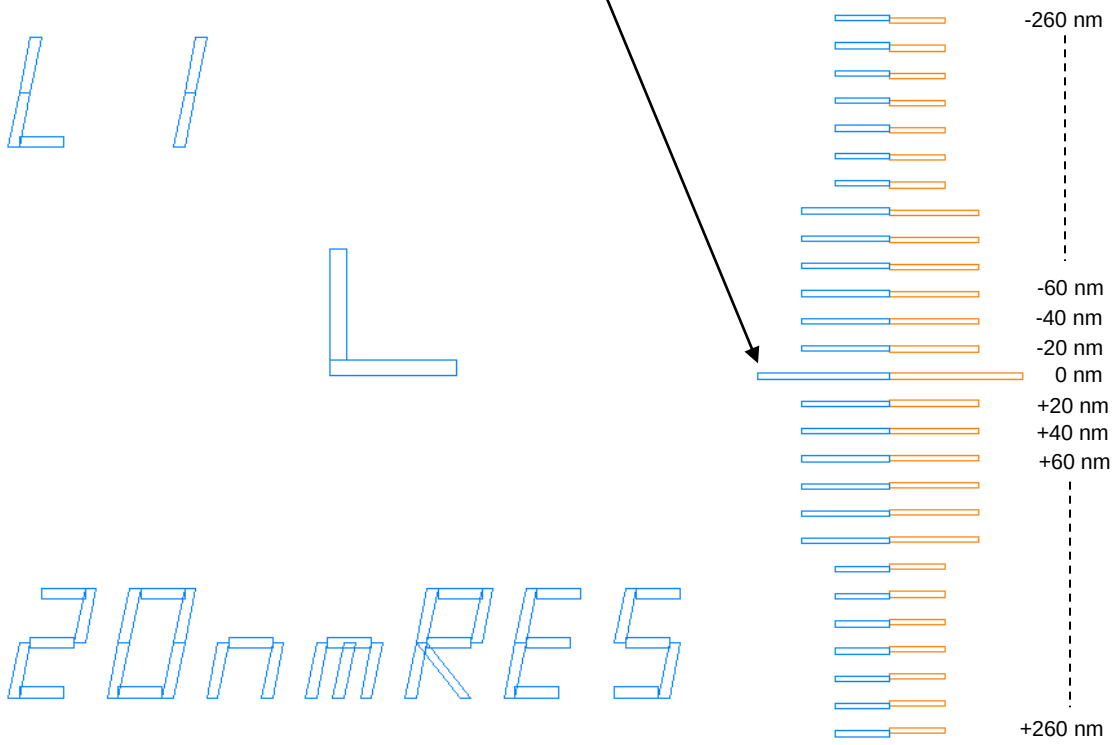


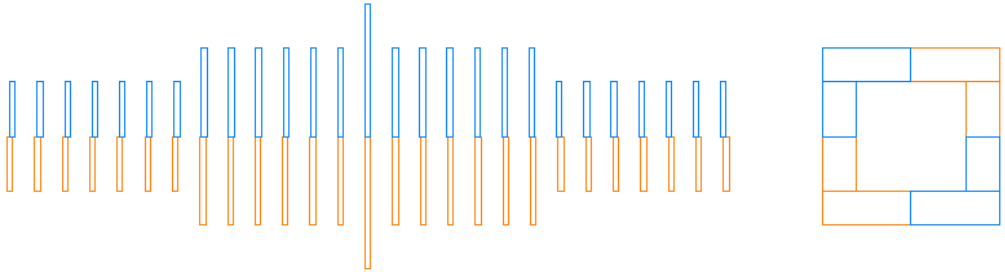
Vernier pattern:

if there is an alignment error, then the amount of errror is indicated by which set of lines are aligned. normally center lines should be aligned.

500 nm lines
2.0 um space

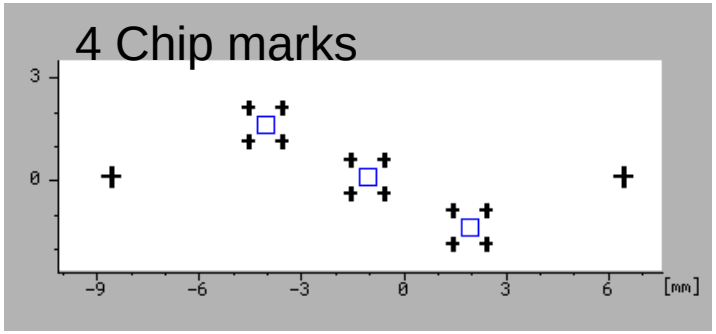


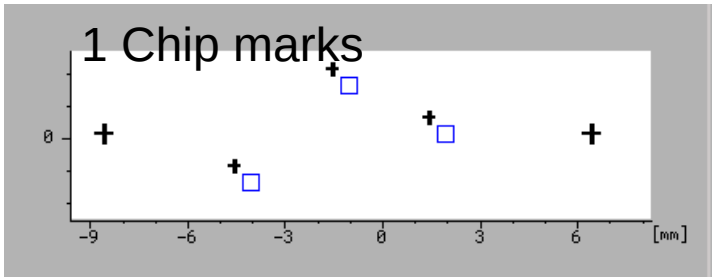
Y offset of orange relative to blue in increments of 20 nm

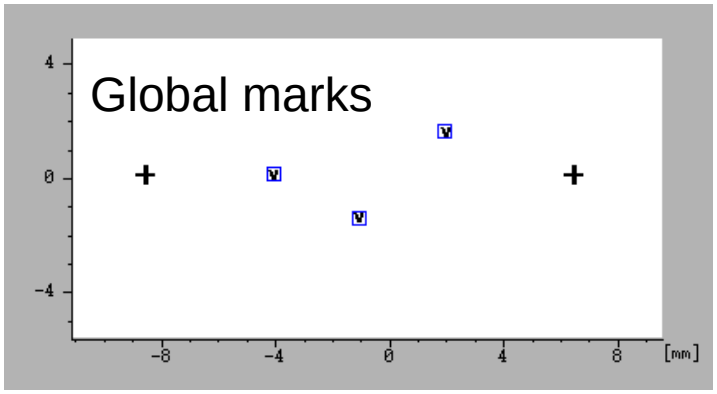


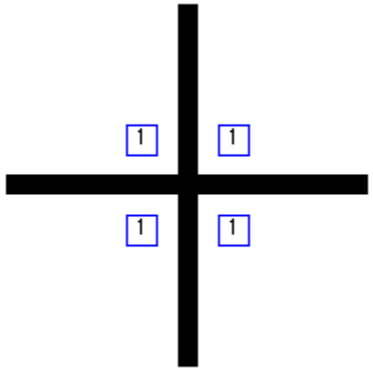
X offset amount is same as Y offset

Pattern Layout





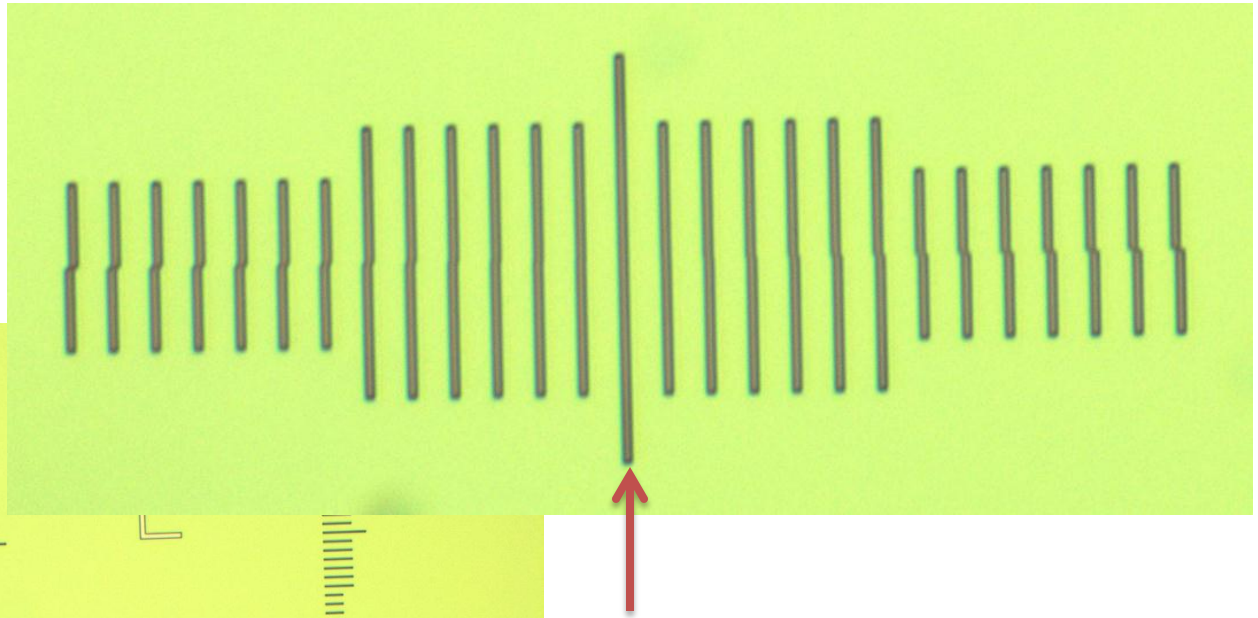


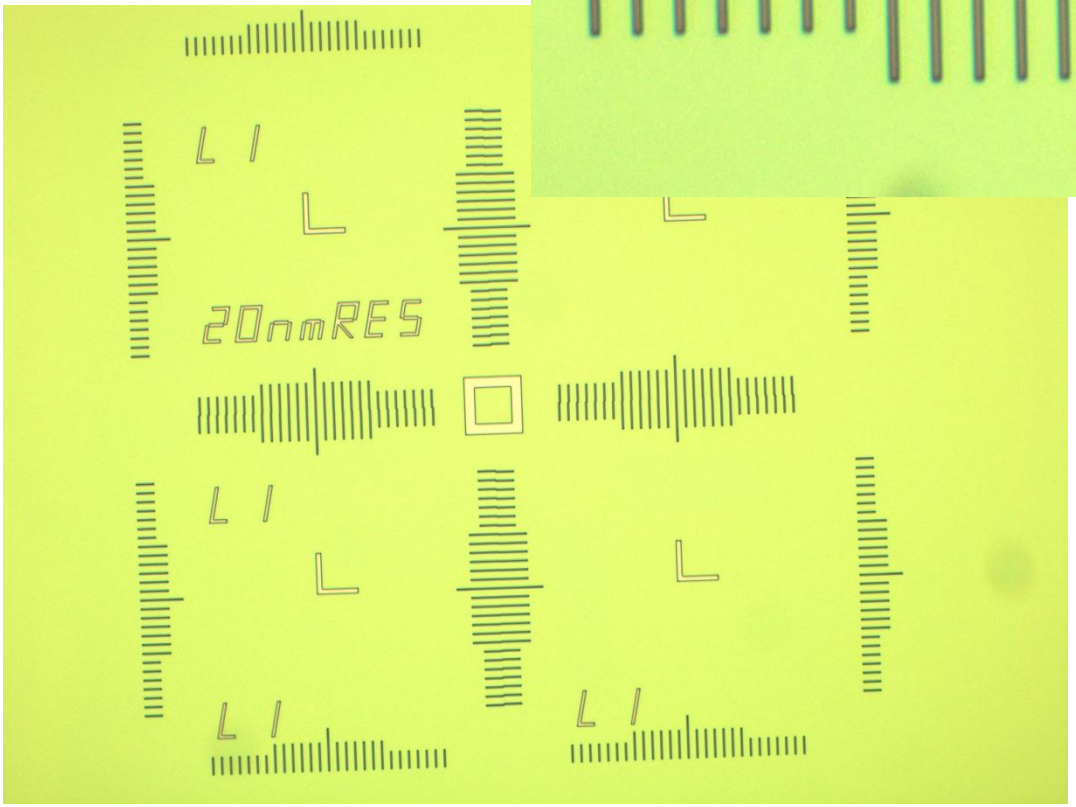


Four 5um squares written around chip mark to ensure not systematic shift from when marks were etched. Alignment done with only global mark detection.

Results from 4 Chip Mark Detection

Alignment with 4 chip marks shows good alignment at center line

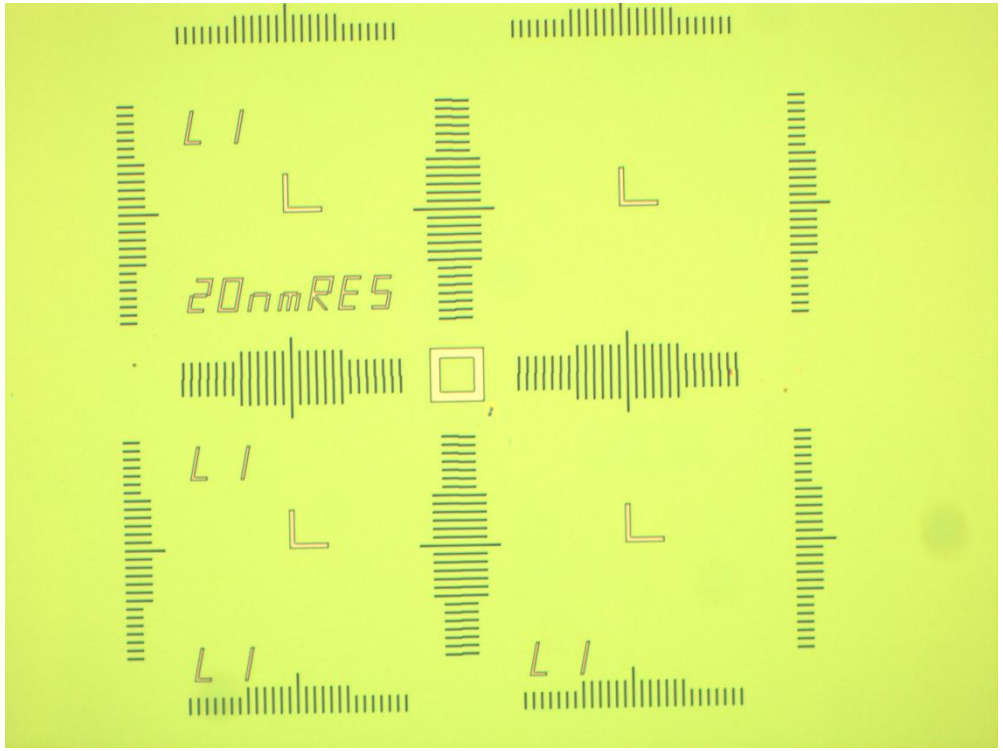


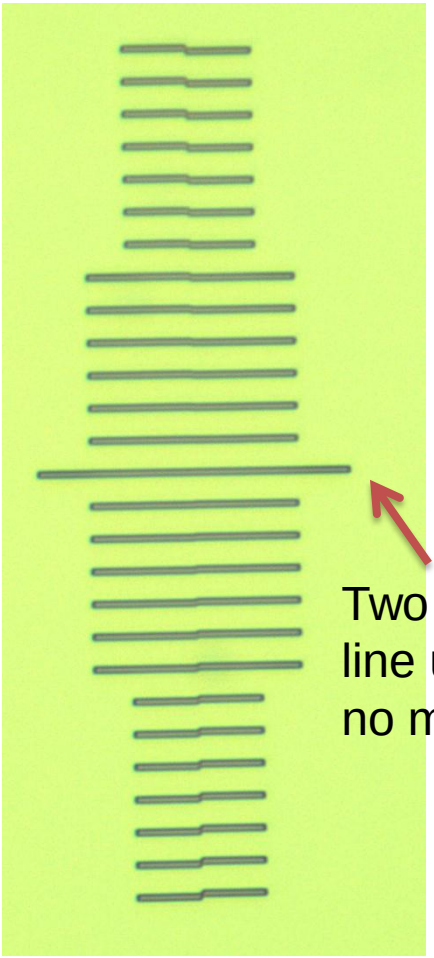


Two center lines line up, so there is no misalignment

Results from 1 Chip Mark Detection

Alignment with 1 chip marks shows good alignment at center line

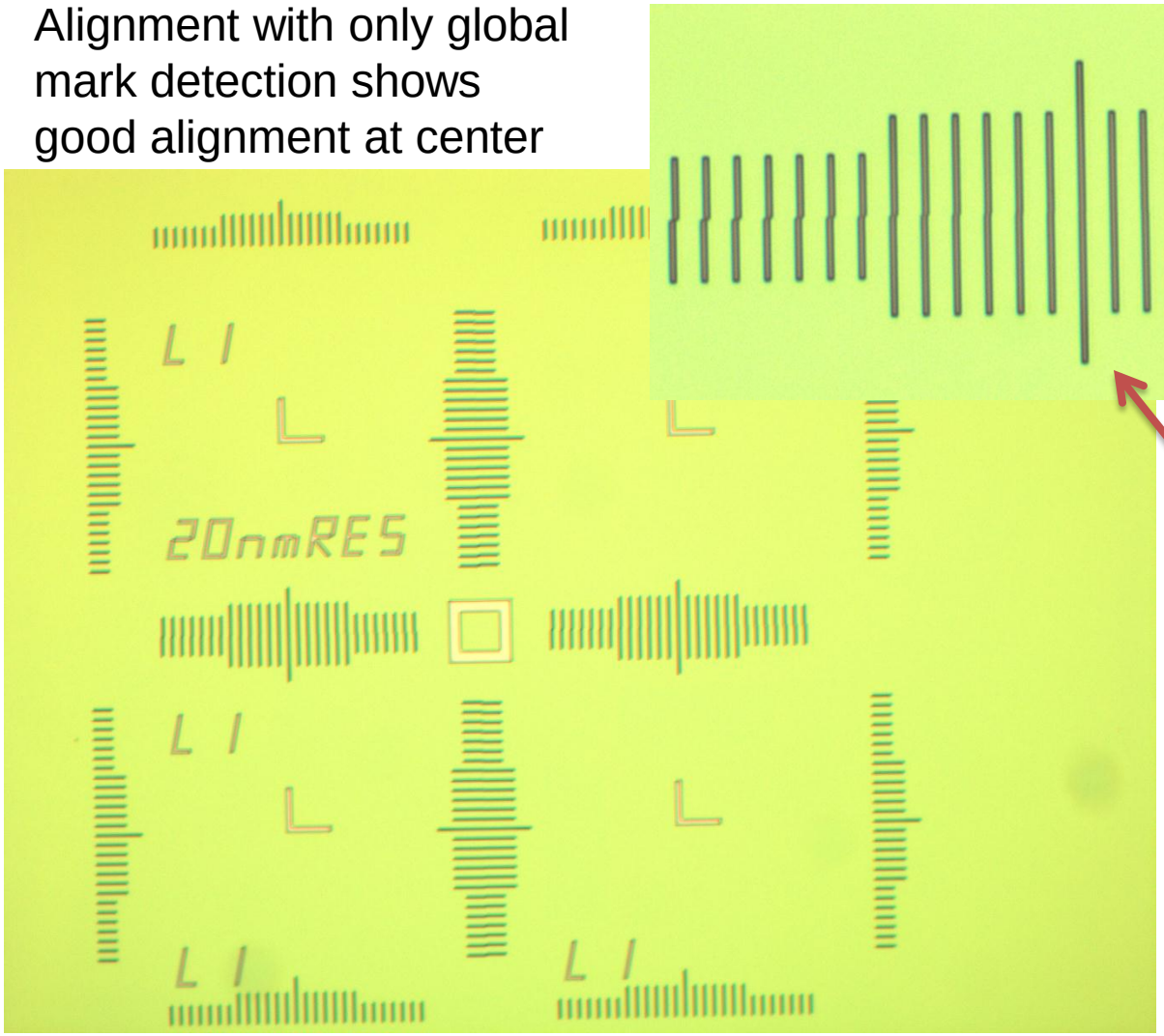




Two center lines line up, so there is no misalignment

Results from Global Mark Detection

Alignment with only global mark detection shows good alignment at center



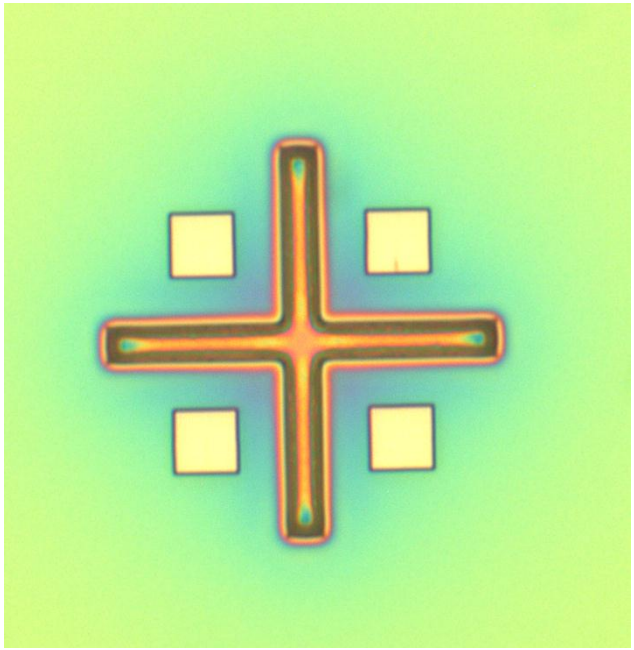
Two center lines line up, so there is no misalignment

Result Summary

		Misalignment (nm)			
Type of Alignment	**Position**	**Upper**	**Left**	**Lower**	**Right**
4 Chipmark Detection	c1r1	10	0	0	0
4 Chipmark Detection	c2r2	20	0	0	10
4 Chipmark Detection	c3r3	10	0	20	0
1 Chipmark Detection	c1r3	20	10	10	0
1 Chipmark Detection	c2r1	10	10	0	0
1 Chipmark Detection	c3r2	20	10	0	0
Global Mark Detection	c1r2	10	0	0	0
Global Mark Detection	c2r3	20	20		
Global Mark Detection	c3r2	10	0	10	20

average	
4 Chipmark Detection	5.83 nm
1 Chipmark Detection	7.50 nm
Global mark detection	9.00 nm

Results of Alignment Around Chip Marks



- 4 squares were written around the chip marks to ensure there was no systematic alignment error.
- Squares should be even spaced away form the cross.
- Looks to be the case.