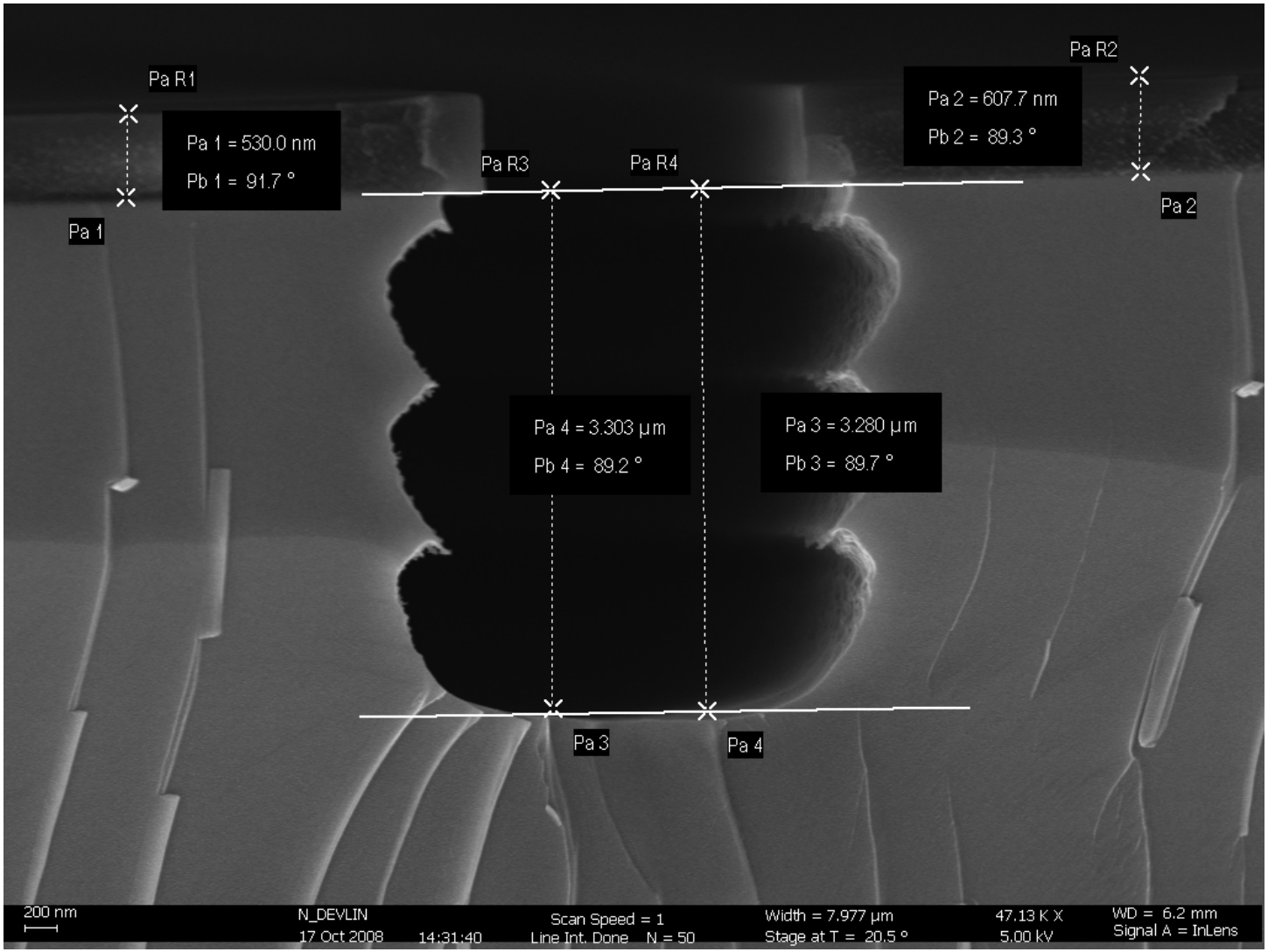
Silicon etching with Bosch process
on
STS ICP

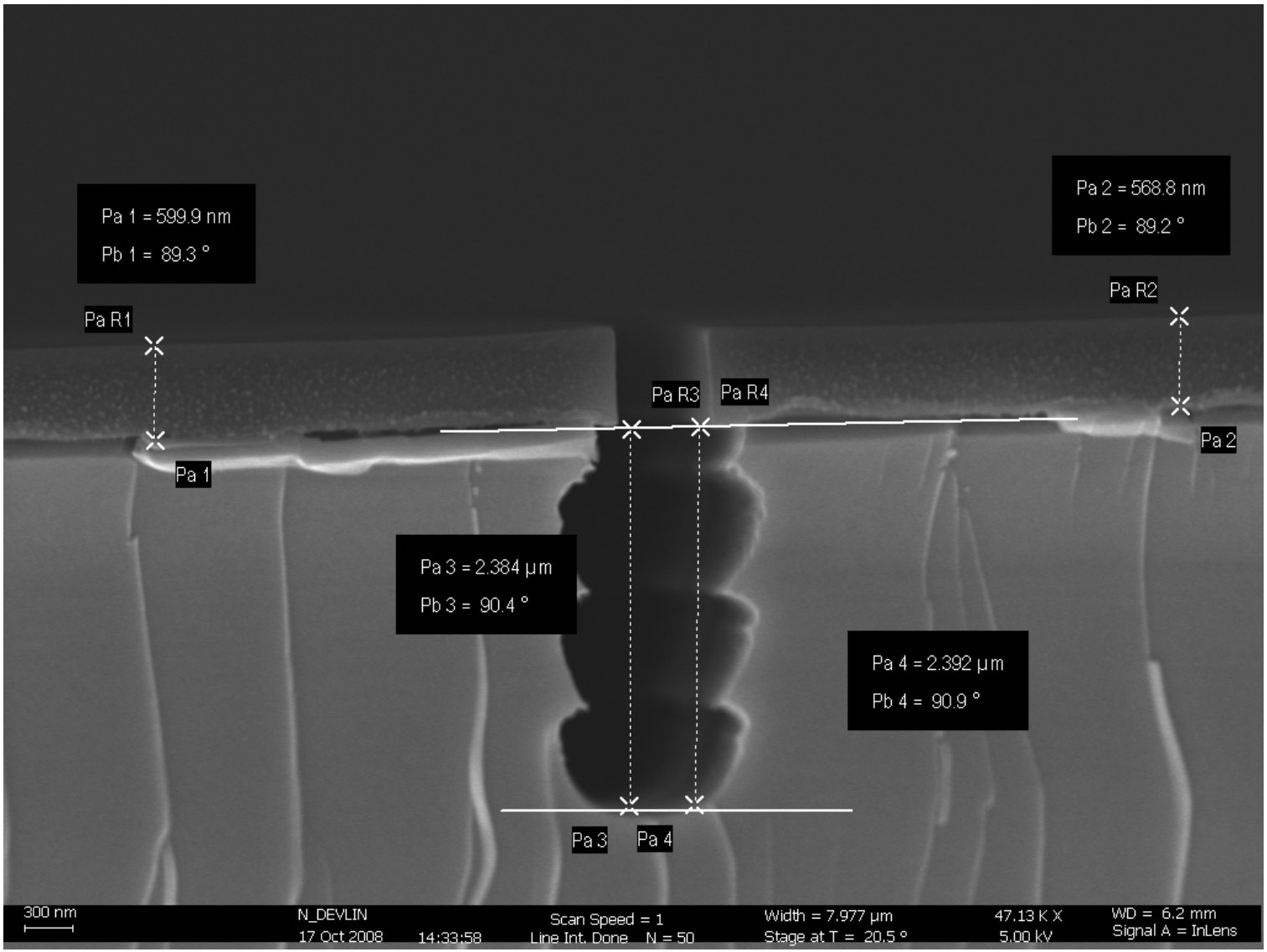
Process Flow

- substrate
  - 4” silicon wafer, 100 orientation
- resist coat
  - ZEP520
  - 1000 RPM, 500 RPM/s, 60 sec
  - 180 C hotplate, 2min
- reflectivity measurement of resist
  - Nanospec, recipe = ZEP on Silicon (10X)
  - mean = 658nm, sigma = 5nm
- EBL expose
  - multiple chips of 3 mm long lines with widths of 2um, 0.5um, and 100nm lines (pk09.mgn)
  - 2nA, 100kV
- develop
  - n-amyl acetate, 2 min immersion
  - IPA immersion, 30 sec
- Silicon etch
  - snap cleave chips into separate pieces
  - mount with cool grease on 4” silicon wafer coated with 1 um oxide
  - STS ICP
  - recipe = wp_high.set
  - target etch rate = 0.6 um / cycle
  - ran for 4 cycles

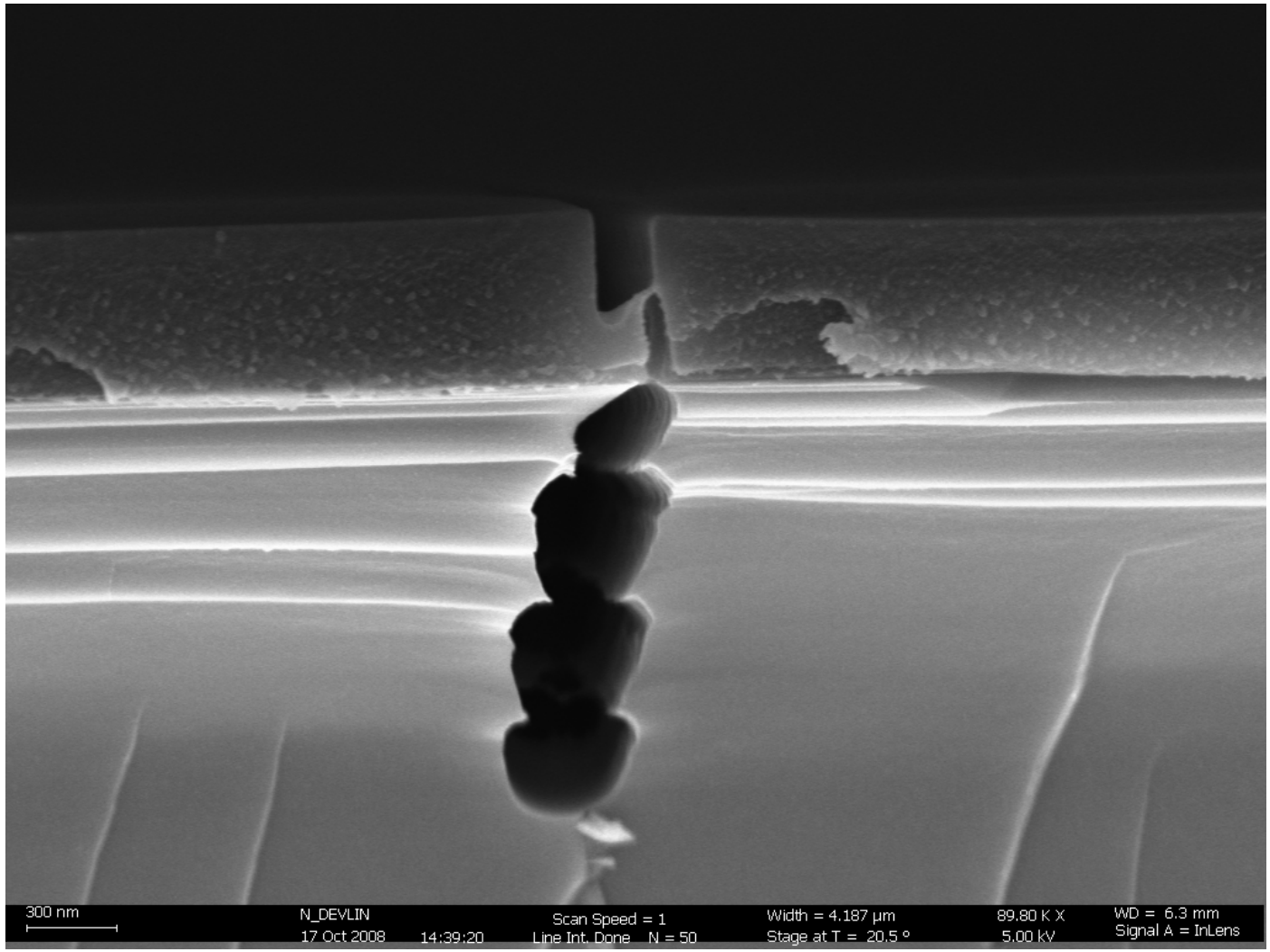
2um line


Pa R1
Pa 1 = 530.0 nm
Pb 1 = 91.7 °
Pa 1
Pa R2
Pa 2 = 607.7 nm
Pb 2 = 89.3 °
Pa 2
Pa R3
Pa R4
Pa 4 = 3.303 µm
Pb 4 = 89.2 °
Pa 3 = 3.280 µm
Pb 3 = 89.7 °
Pa 3
Pa 4
200 nm
N_DEVLIN
17 Oct 2008
14:31:40
Scan Speed = 1
Line Int. Done N = 50
Width = 7.977 µm
Stage at T = 20.5 °
47.13 K X
5.00 kV
WD = 6.2 mm
Signal A = InLens

0.5um line


Pa 1 = 599.9 nm
Pb 1 = 89.3 °
Pa 2 = 568.8 nm
Pb 2 = 89.2 °
Pa R1
Pa R2
Pa R3
Pa R4
Pa 1
Pa 2
Pa 3 = 2.384 µm
Pb 3 = 90.4 °
Pa 4 = 2.392 µm
Pb 4 = 90.9 °
Pa 3
Pa 4
300 nm
N_DEVLIN
17 Oct 2008
14:33:58
Scan Speed = 1
Line Int. Done N = 50
Width = 7.977 µm
Stage at T = 20.5 °
47.13 K X
5.00 kV
WD = 6.2 mm
Signal A = InLens

100nm line


300 nm
N_DEVLIN
17 Oct 2008
14:39:20
Scan Speed = 1
Line Int. Done N = 50
Width = 4.187 µm
Stage at T = 20.5 °
89.80 K X
5.00 kV
WD = 6.3 mm
Signal A = InLens