Si etching with ZEP520A resist and oxide hard mask

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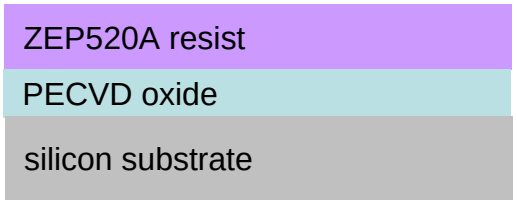
Summary

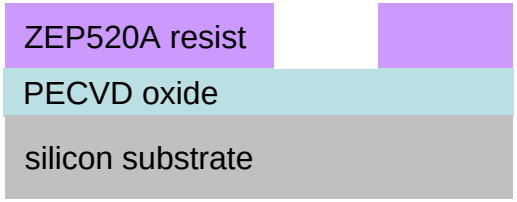
- ZEP520A typically has a 1:1 dry plasma etch selectivity relative to Si and SiO2
- required lateral pattern dimensions usually restrict ZEP520A thickness to less than 600nm
- if more than 600nm of Si or SiO2 is desired to be etched, then 600nm of ZEP20A will be insufficient
- this summary shows how an SiO2 "hard mask" can be used to etch Silicon to depths beyond what would be possible with ZEP520A alone

Process Flow

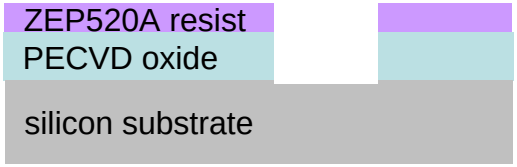
1. resist coat



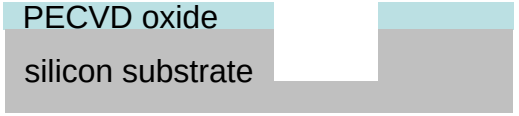
2. EBL expose/develop



3. SiO2 hard mask etch



4. Si etch

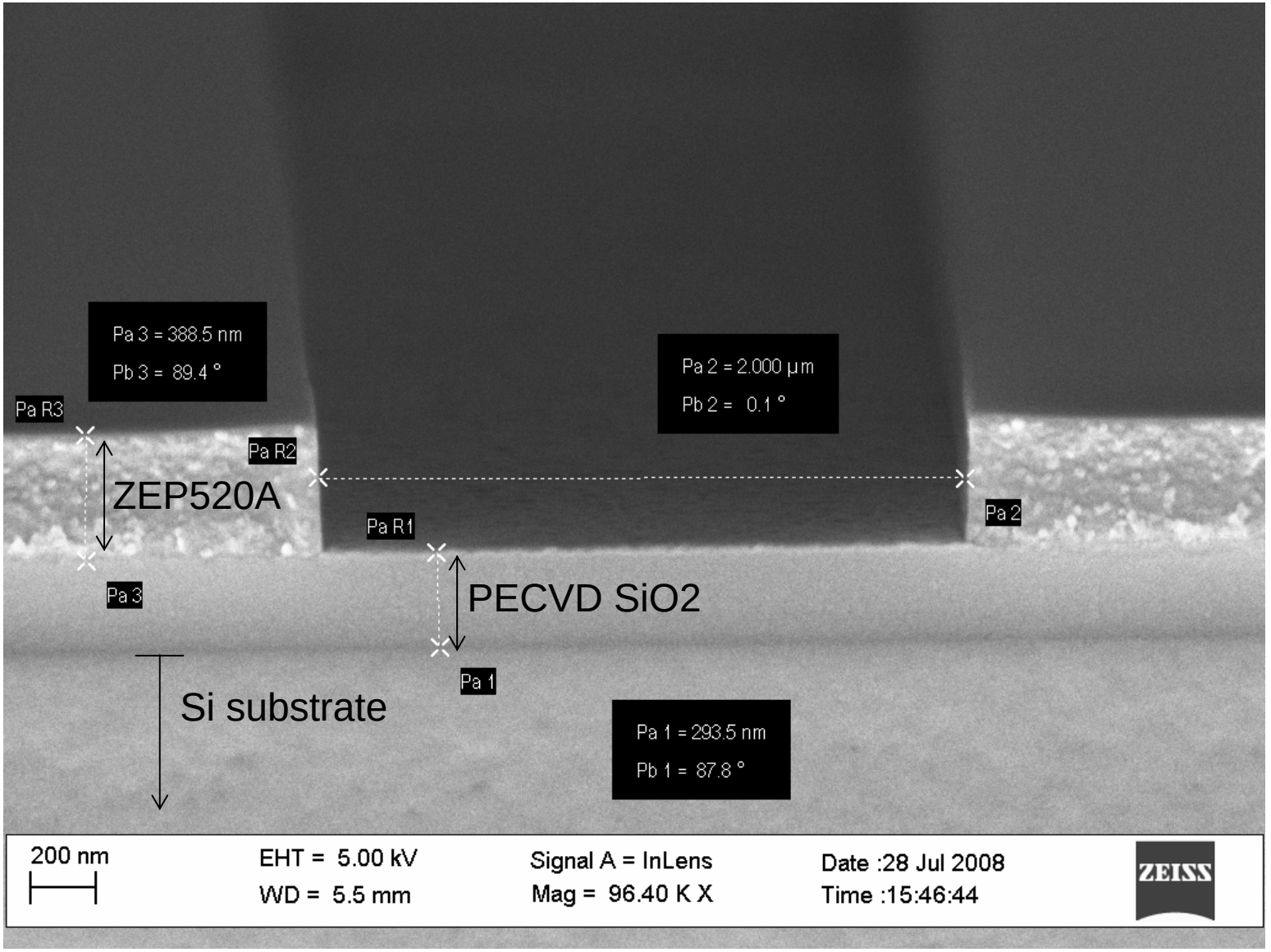


Process Flow

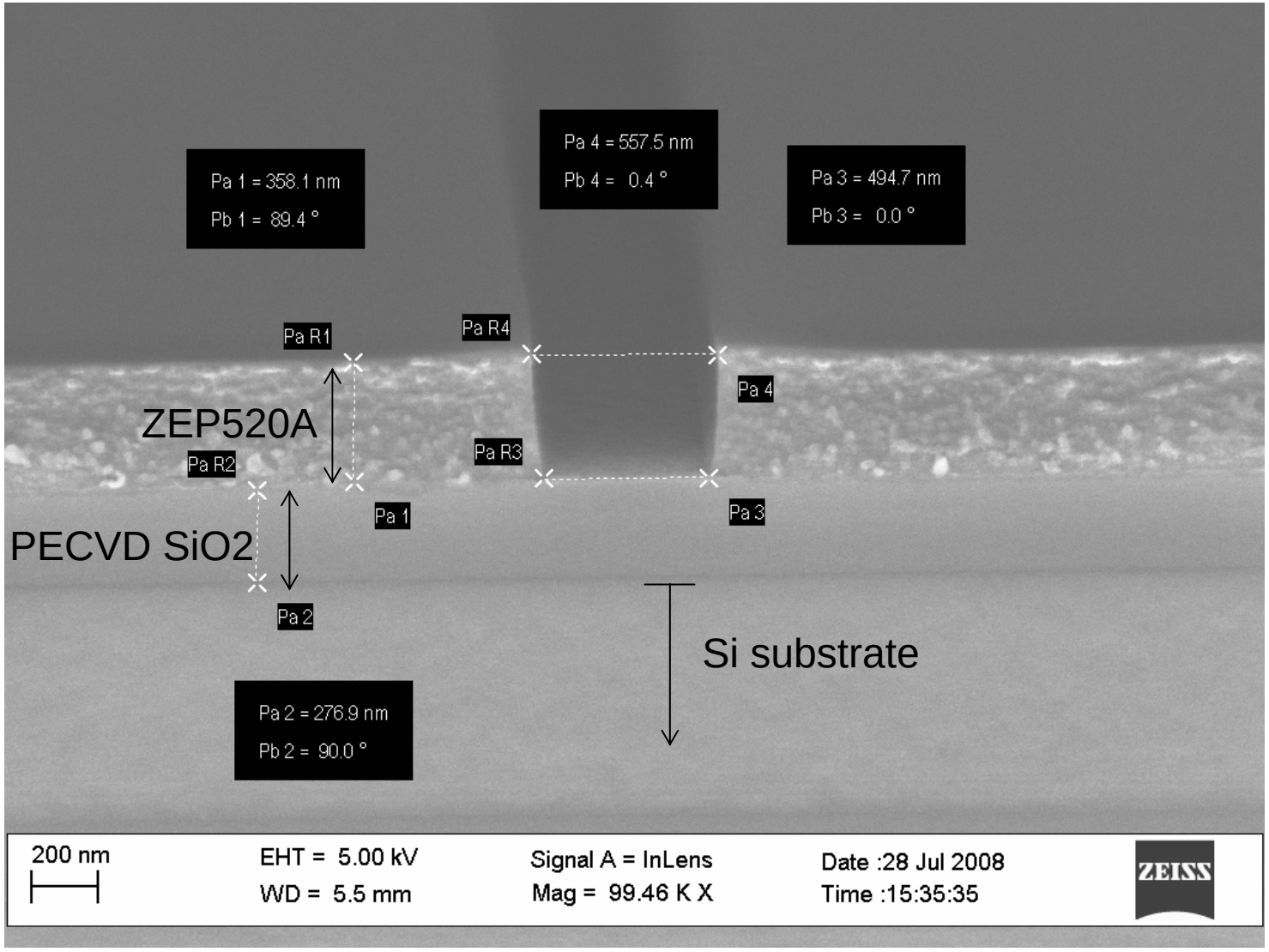
- PECVD oxide dep
- Resist Coat
  - ZEP520A
- EBL exposure
  - 100kV, 2nA
- Resist Develop
  - 2min immersion n-Amyl Acetate, 30sec immersion IPA rinse
- SiO2 etch
  - Plasma Therm ICP
  - 5mTorr, 25sccm C4F6, 15sccm CF4, 4sccm Ar, 4sccm O2, RF1 = 400W, RF2 = 400W
- Si etch
  - STS SOE ICP
  - 5mTorr, 20sccm Cl2, 5sccm Ar, coil = 600W, plate = 50W

Post expose/develop

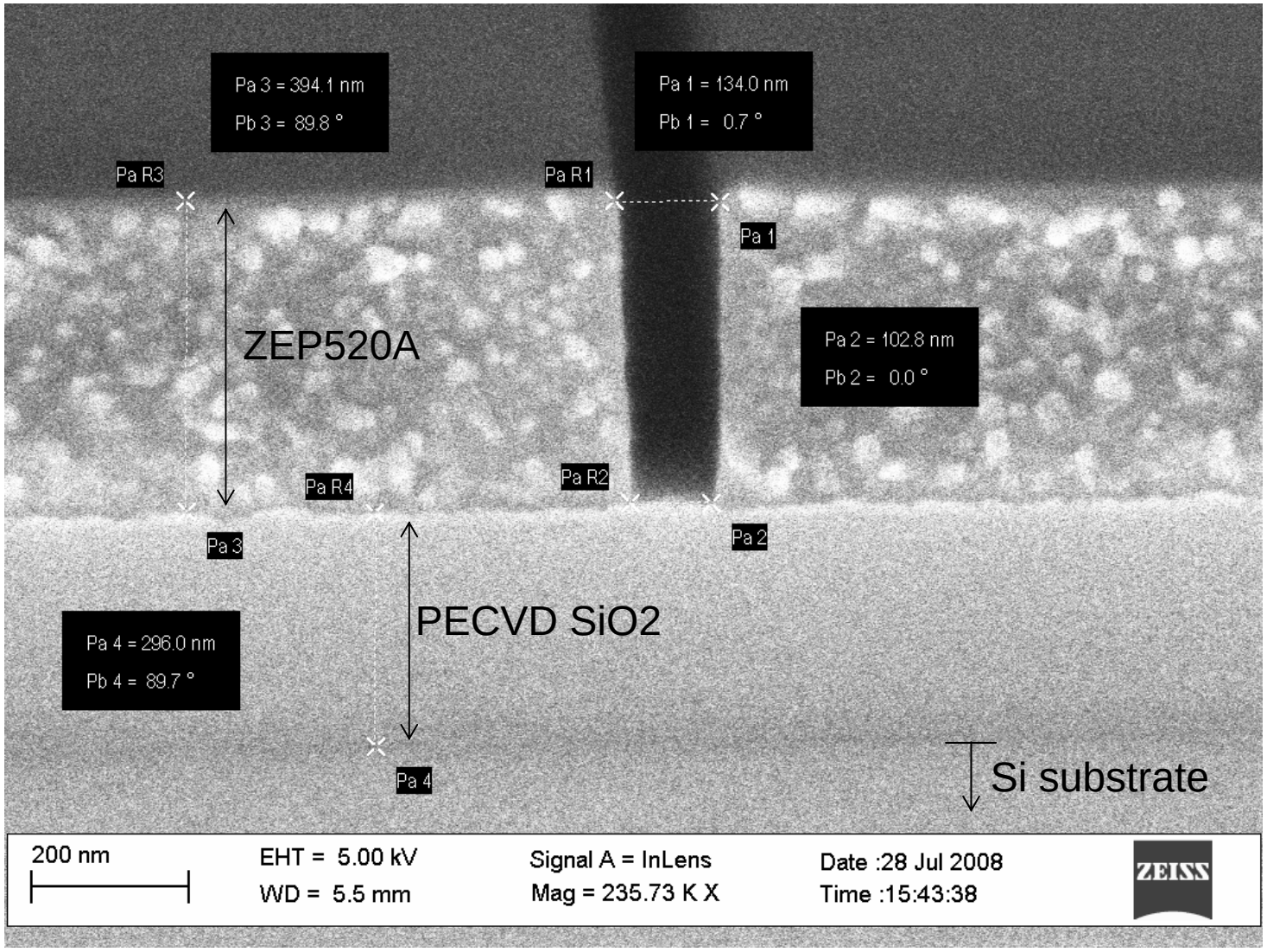
2um line post expose/develop



0.5um line post expose/develop

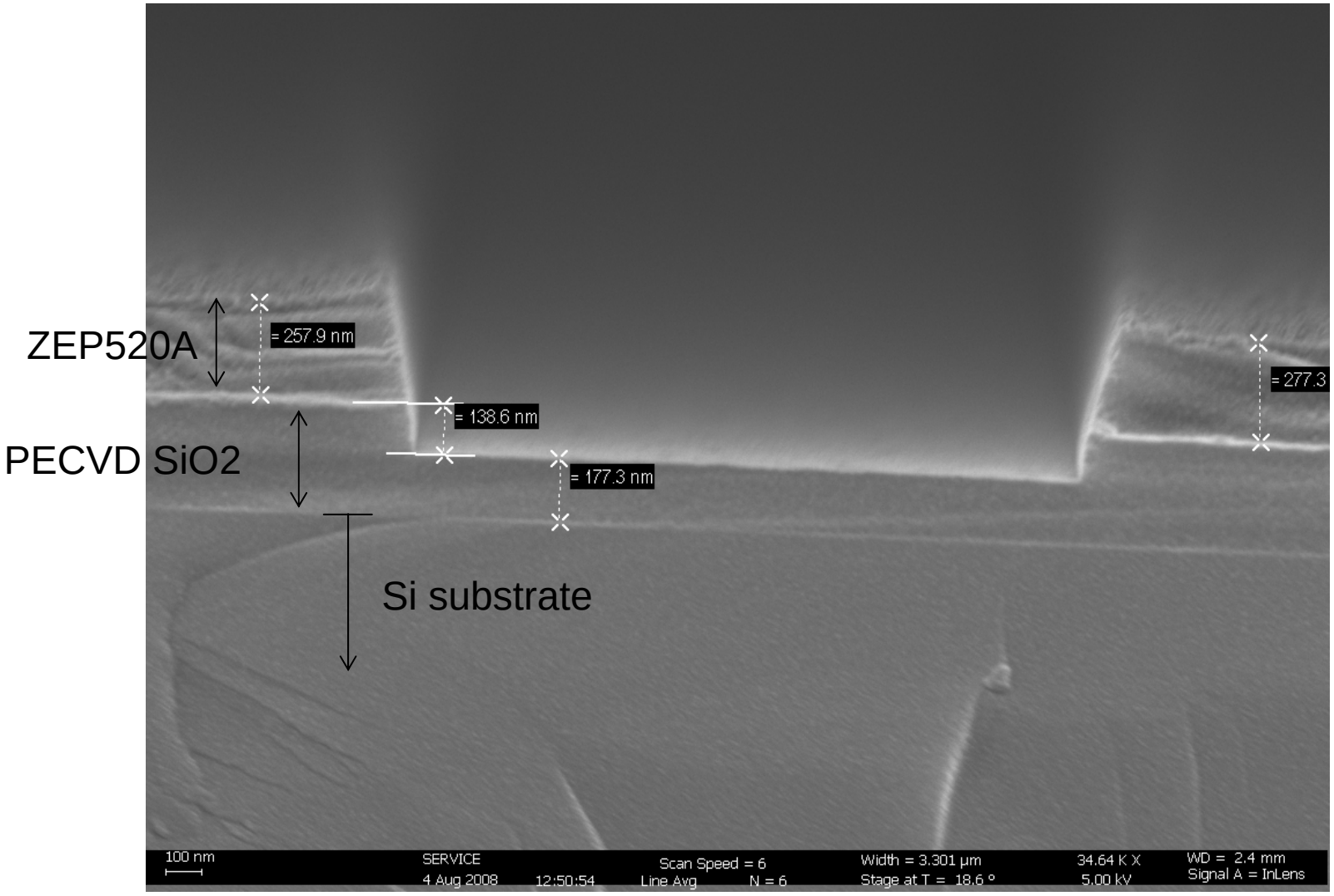


100nm line post expose/develop

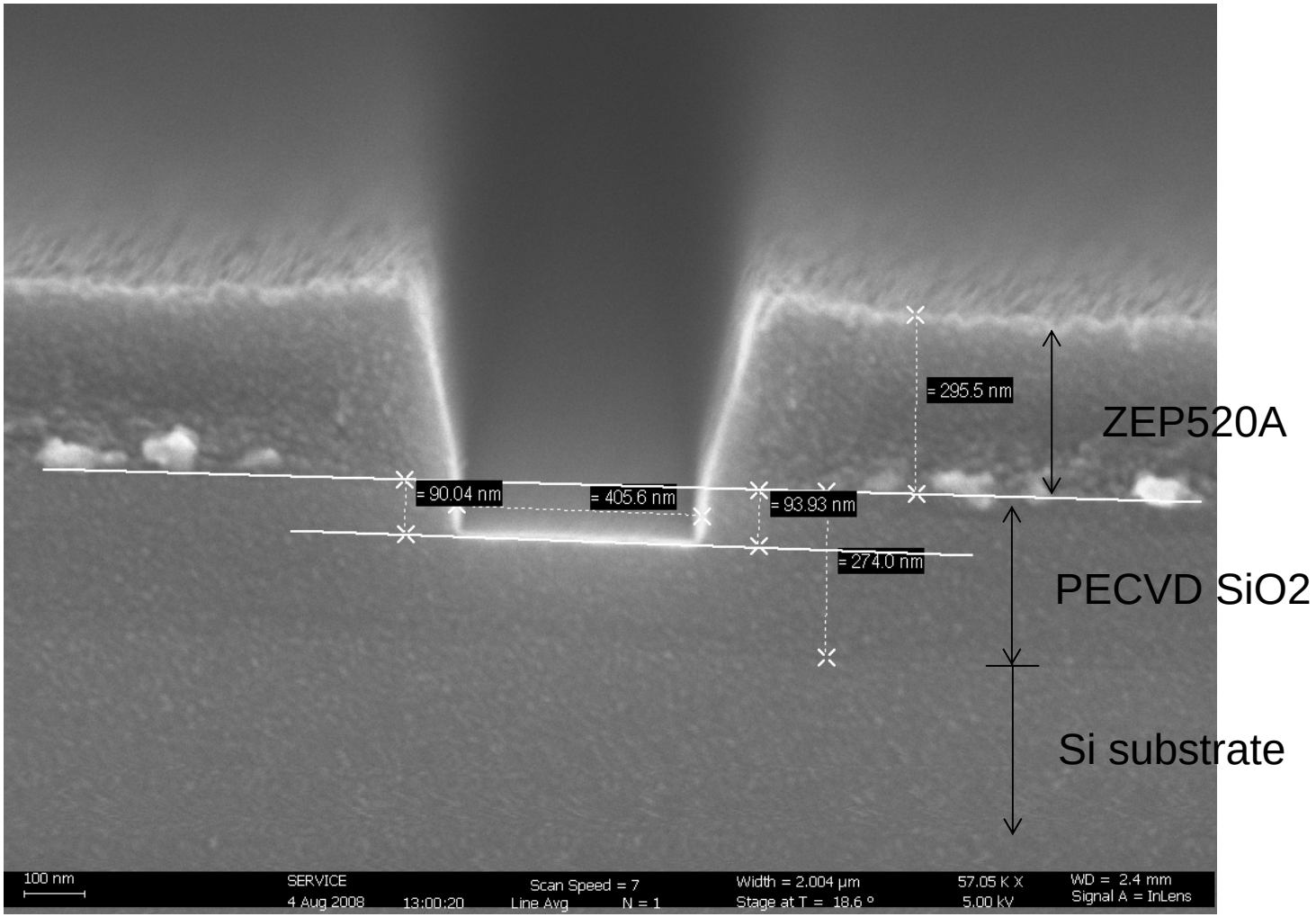


Post partial SiO2 etch

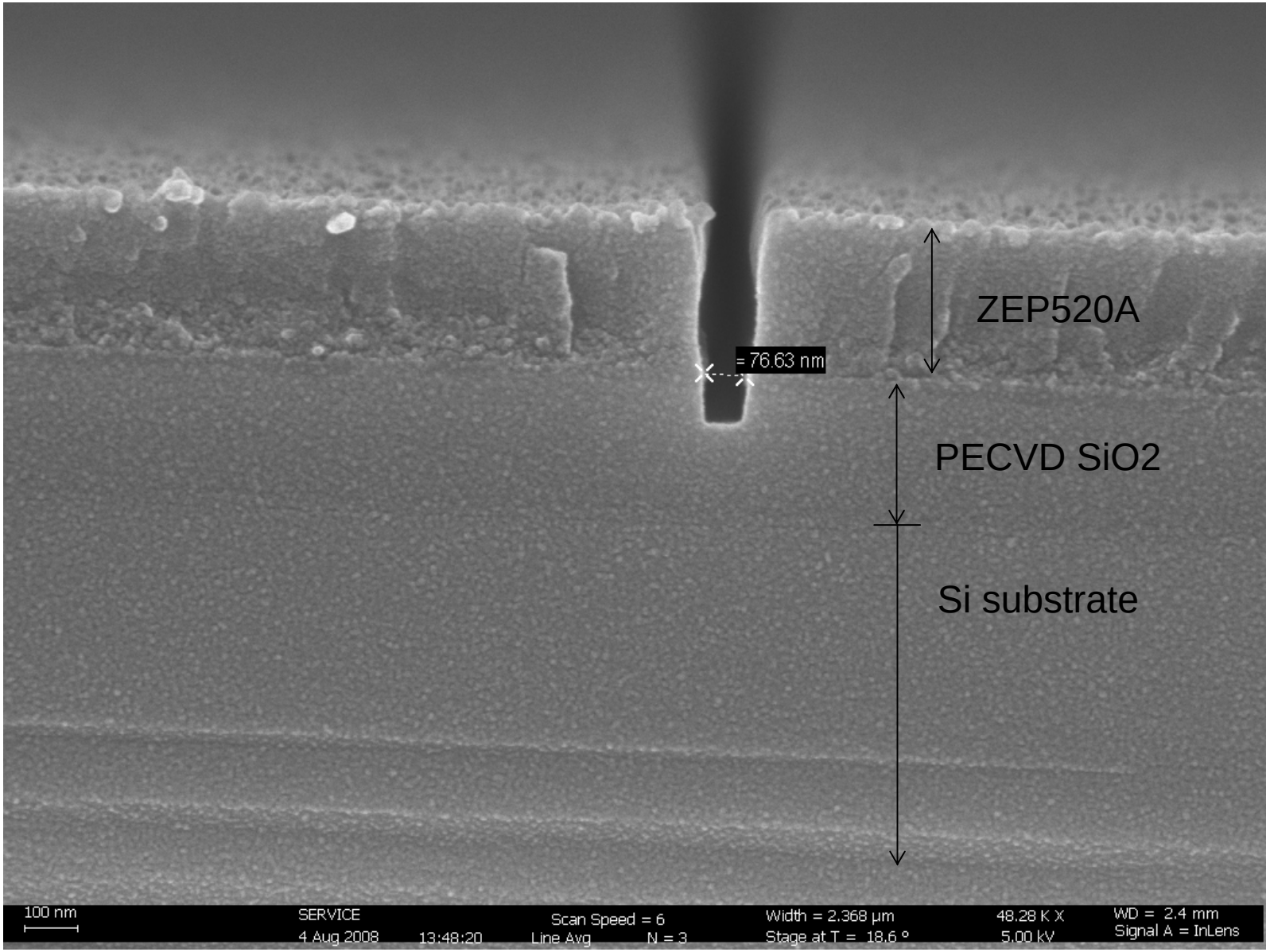
2um line post 30sec SiO2 etch



0.5um line post 30sec SiO2 etch



100nm line post 30sec SiO2 etch



Post expose/develop and before etch

parameter	data
PECVD oxide thickness	mean = 293nm, st dev = 14nm, N = 8
ZEP520A resist thickness	mean = 389nm, st dev = 4nm, N = 3

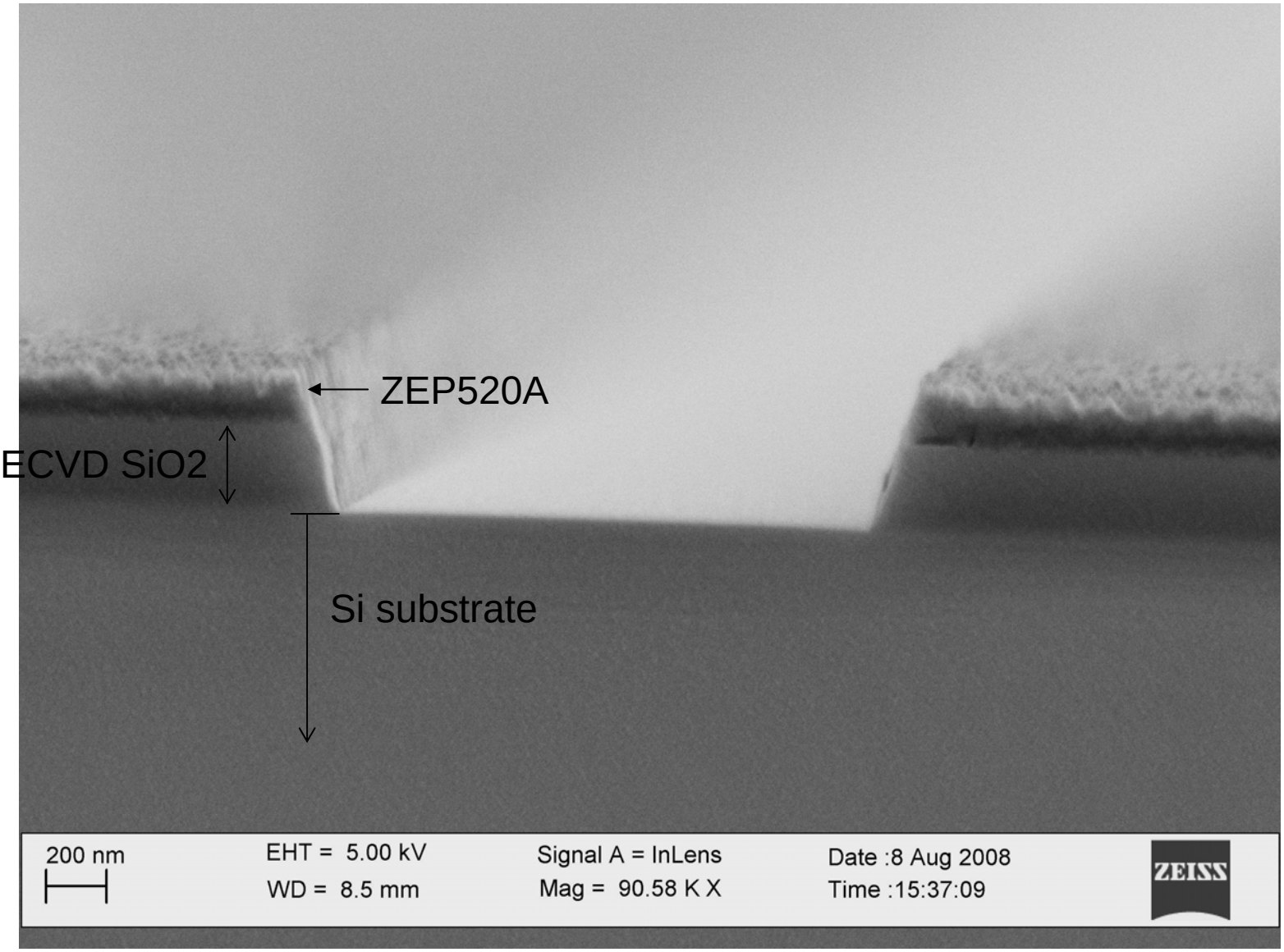
After 30sec of SiO2 etch

parameter	data
PECVD oxide thickness etched	mean = 116nm, st dev = 16nm, N = 5
PECVD oxide etch rate	**3.9nm/s**
ZEP520A resist thickness remaining	mean = 286nm, st dev = 21nm, N = 5
ZEP520 resist etch rate	**3.4nm/s**
selectivity **PECVD oxide : ZEP520**	**1.1 : 1**

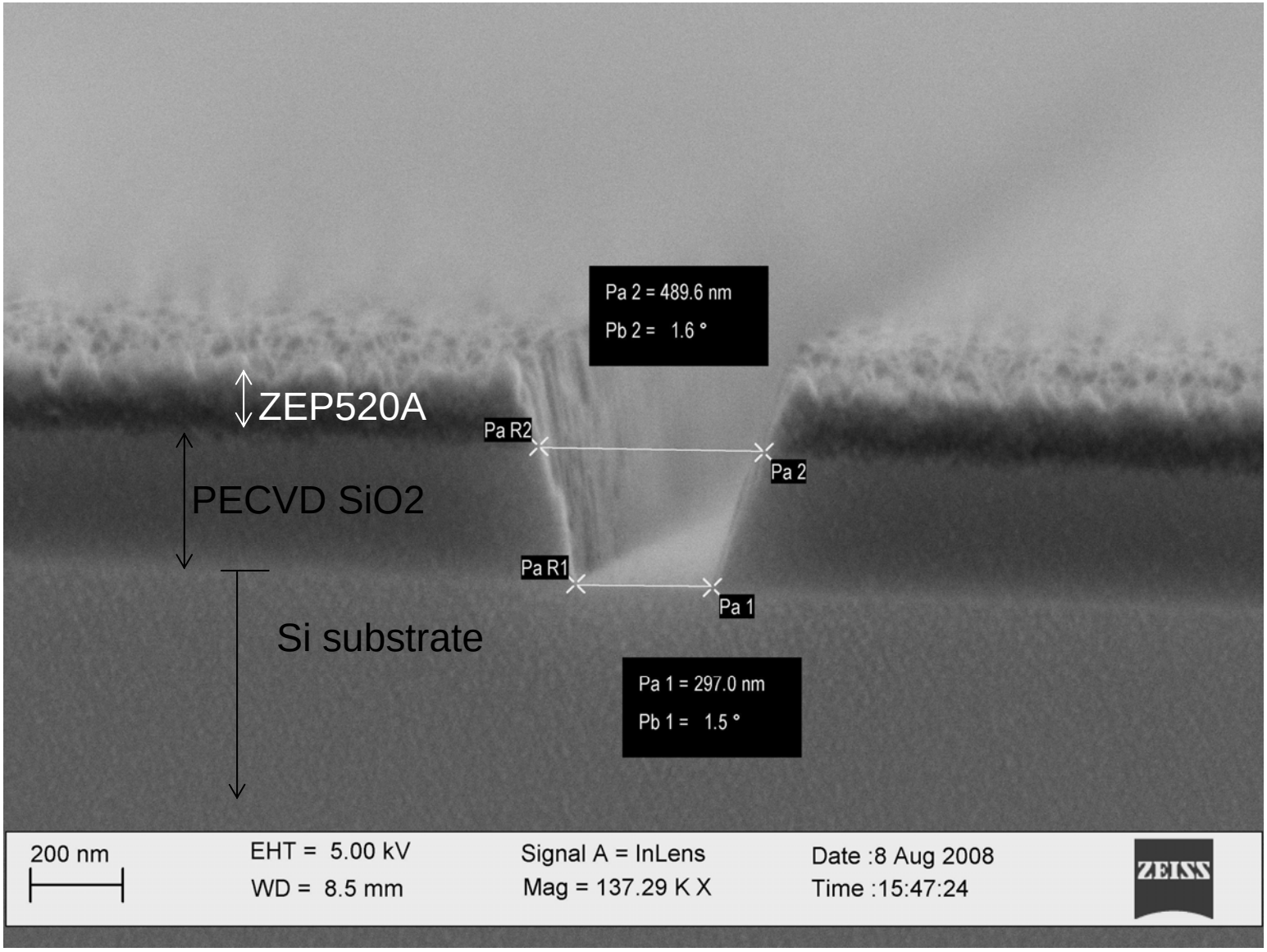
time required to fully etch 293nm of PECVD oxide + 10% overetch = 83sec
(slides that follow show SiO2 fully etched at 83sec)

Post full SiO2 etch

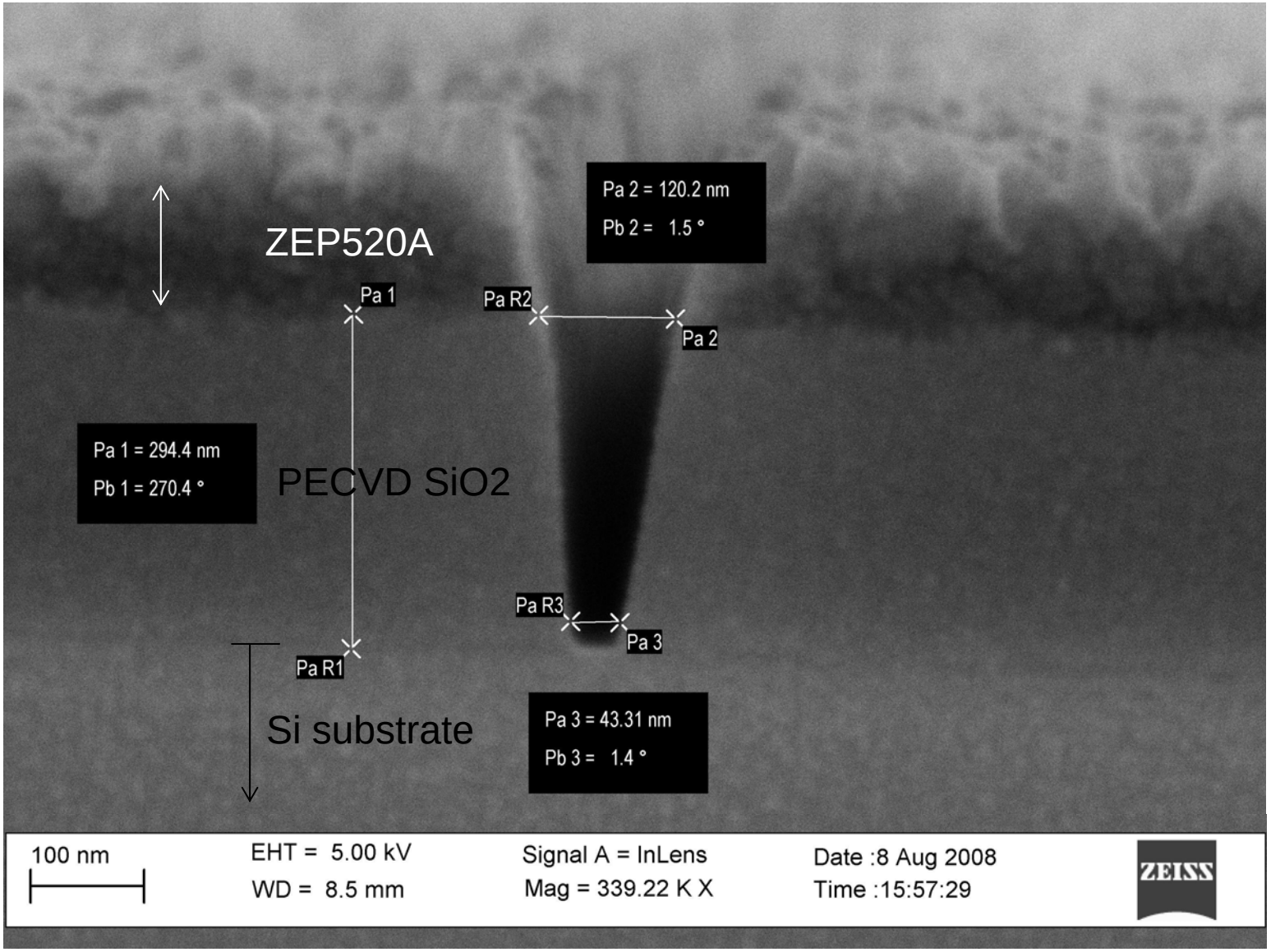
2um line post 83sec SiO2 etch



0.5um line post 83sec SiO2 etch

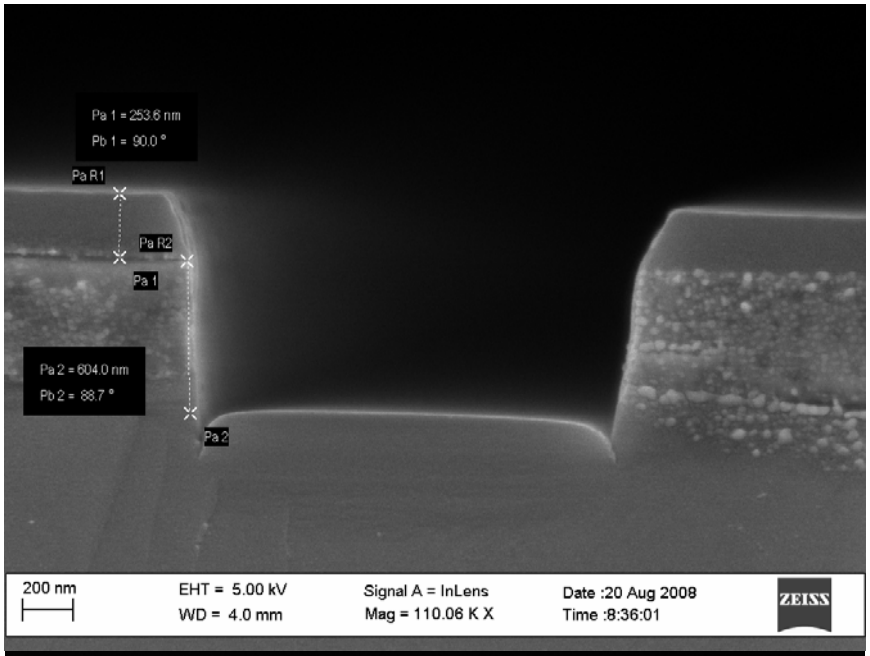


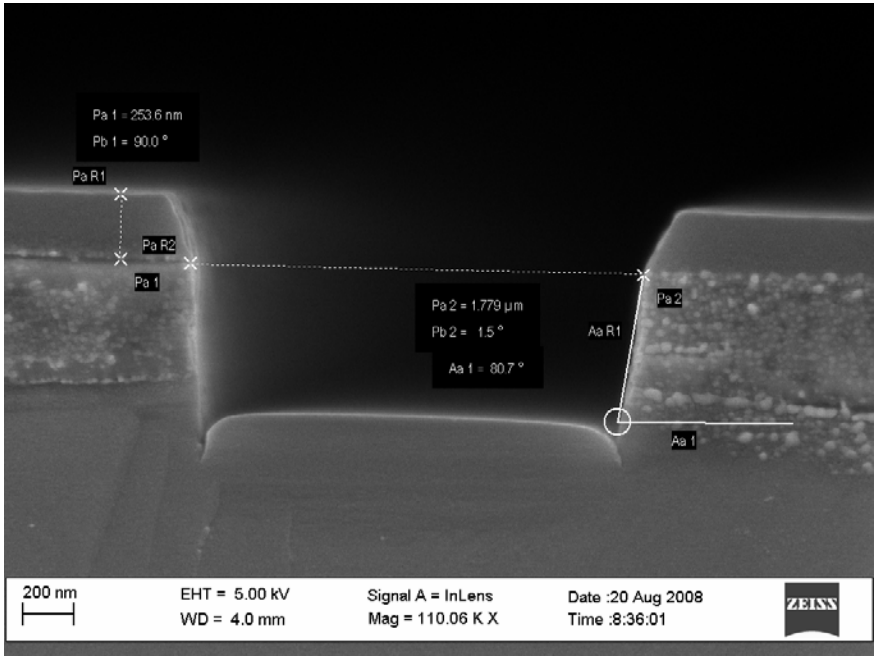
100nm line post 83sec SiO2 etch

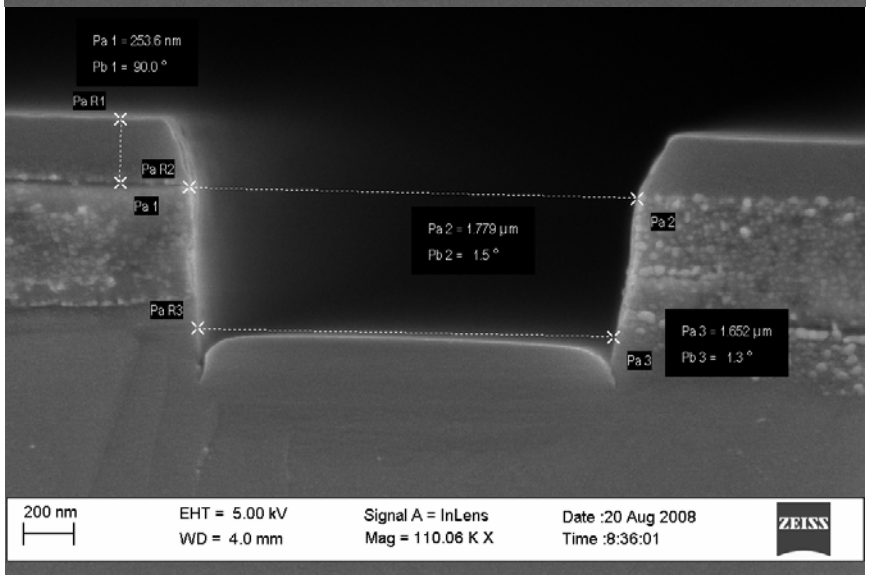


Post partial Si etch
(resist was not removed)

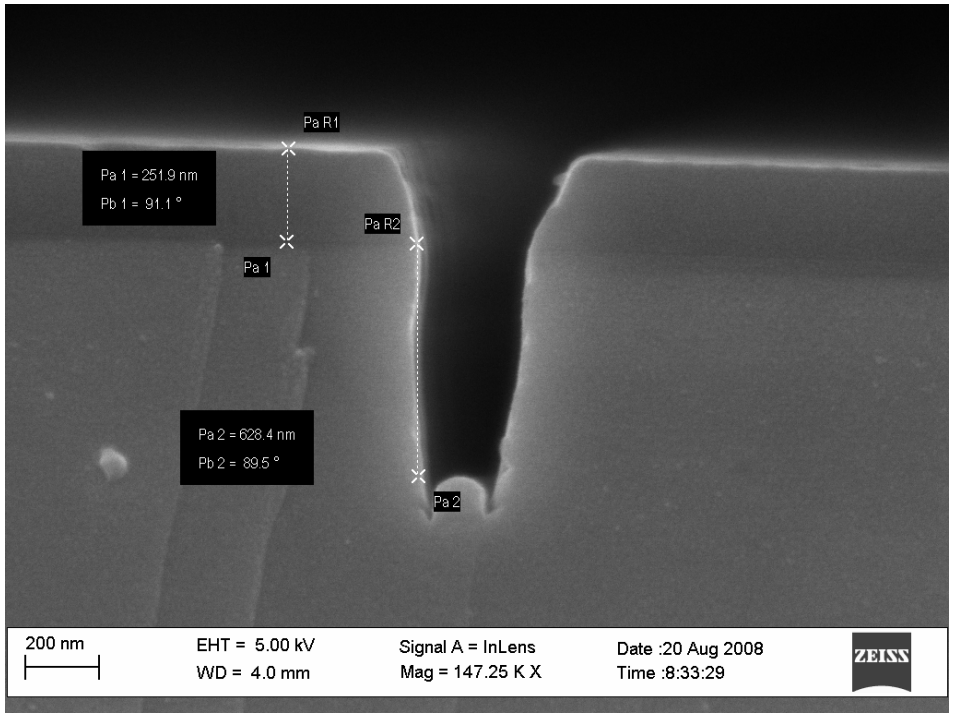
2um line post 120sec Si etch

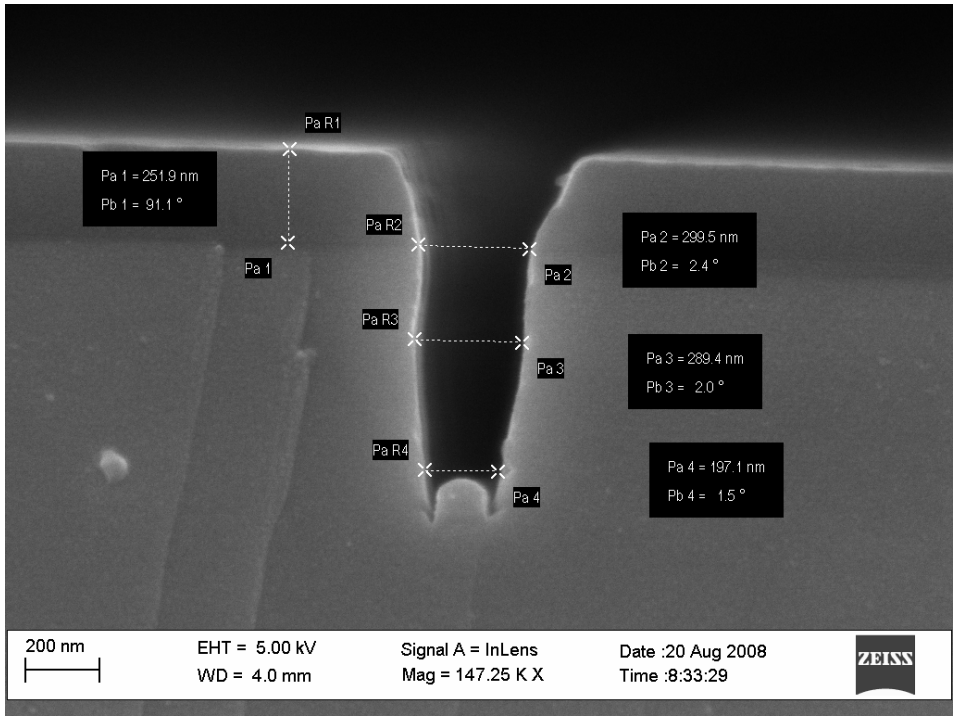




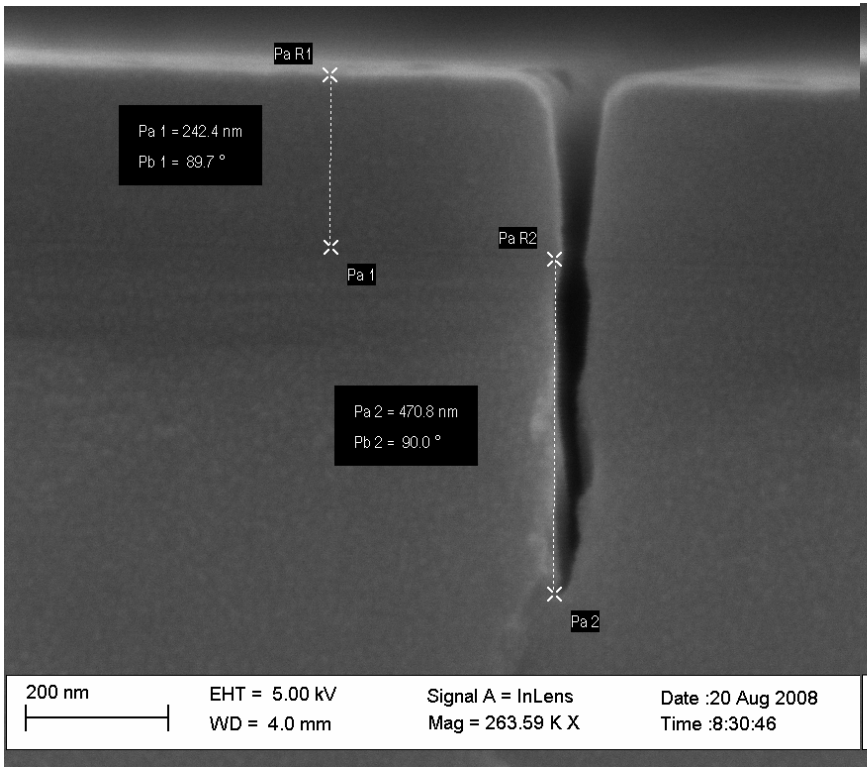


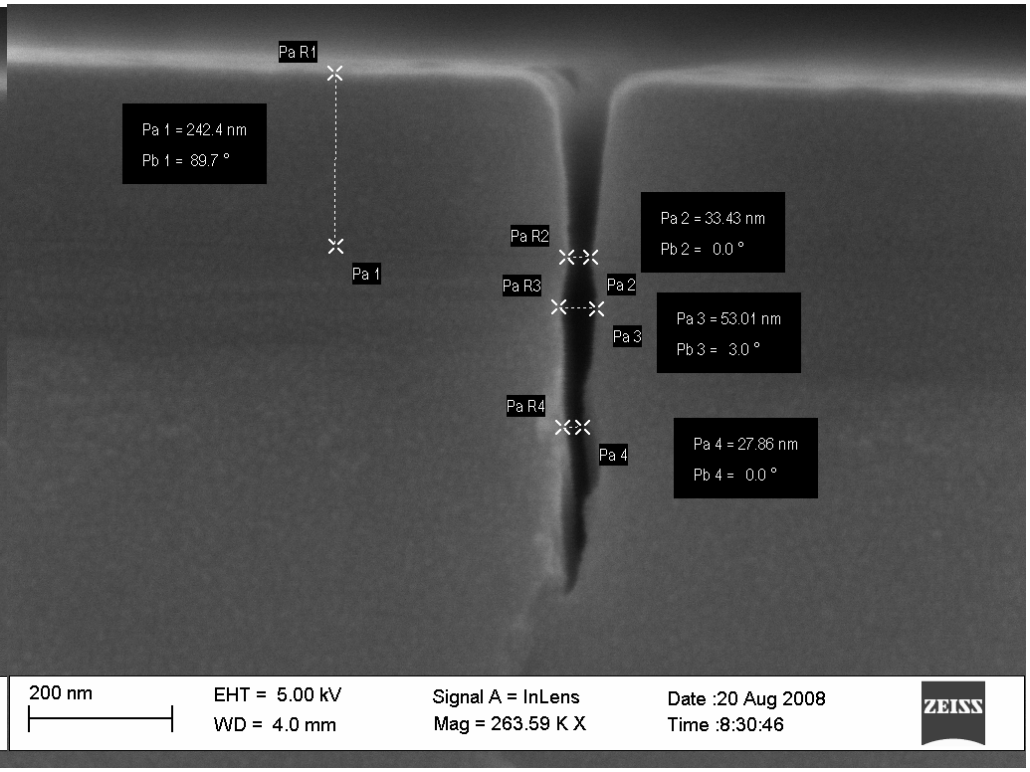
0.5um line post 120sec Si etch





100nm line post 120sec Si etch





After 120sec of Si etch

Resist was not removed after SiO2 etch and prior to Si etch, because it can help provide some small extra buffer for Si etching. The etch rate of resist with the DEVIN1.SET recipe is known to be ~4.6nm/sec. Prior to this etch, there was 139nm of resist still remaining. So, after 30sec, the 139nm of resist will be gone, and then the oxide mask layer will be exposed. The data in the table summarizes the etch parameters.

parameter	data
PECVD oxide thickness etched	mean = 41nm, st dev = 6nm, N = 8
PECVD oxide etch rate	**0.45nm/s**

	2um line	500nm line	100nm line
silicon etched	mean = 599nm sigma = 7nm N = 2	mean = 625nm sigma = 5nm N = 2	mean = 493nm sigma = 19nm N = 3
silicon etch rate	5.0nm/s	5.2nm/s	4.1nm/s
selectivity to oxide	11.1	11.6	9.1

note: sample size is small, don't expect 2um line to etch more slowly than 500nm line