

Silicon ICP etching with HSQ resist

Devin K. Brown, Georgia Tech

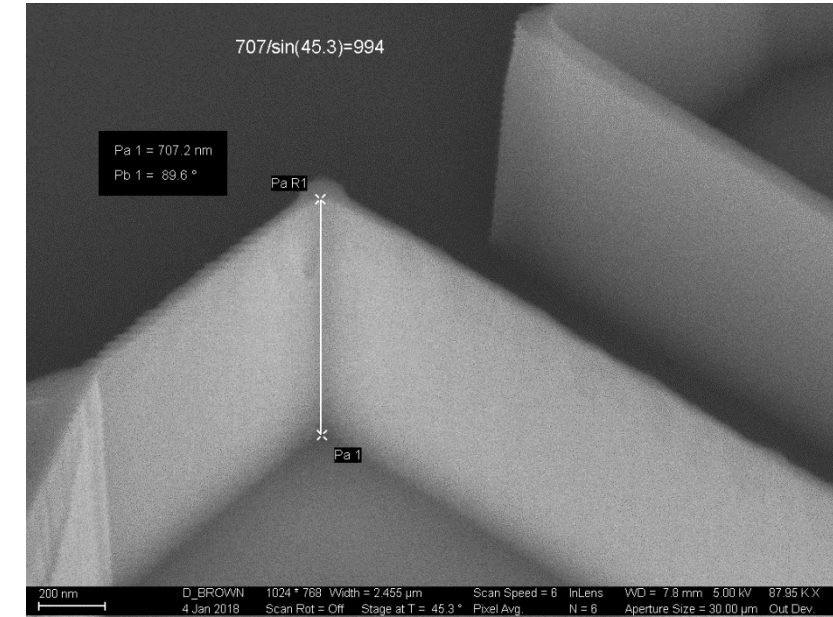
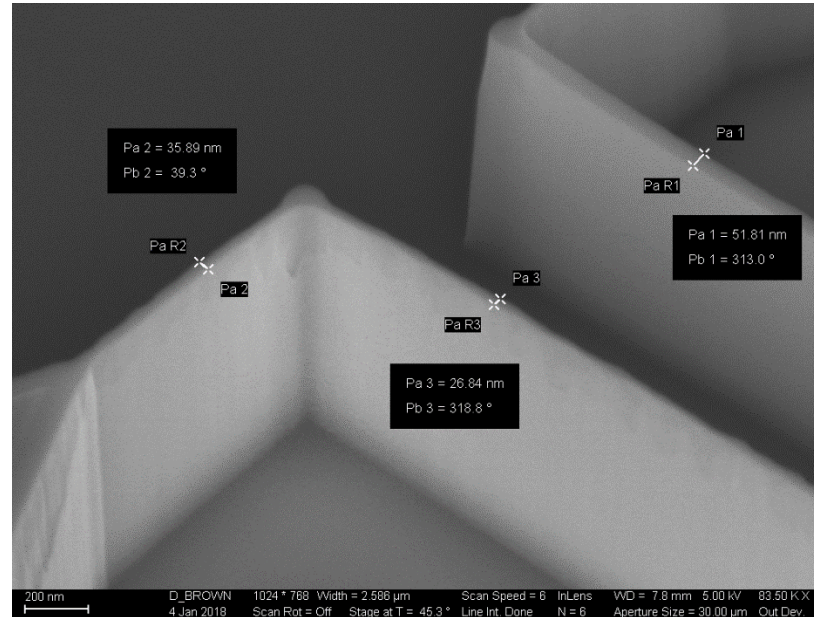
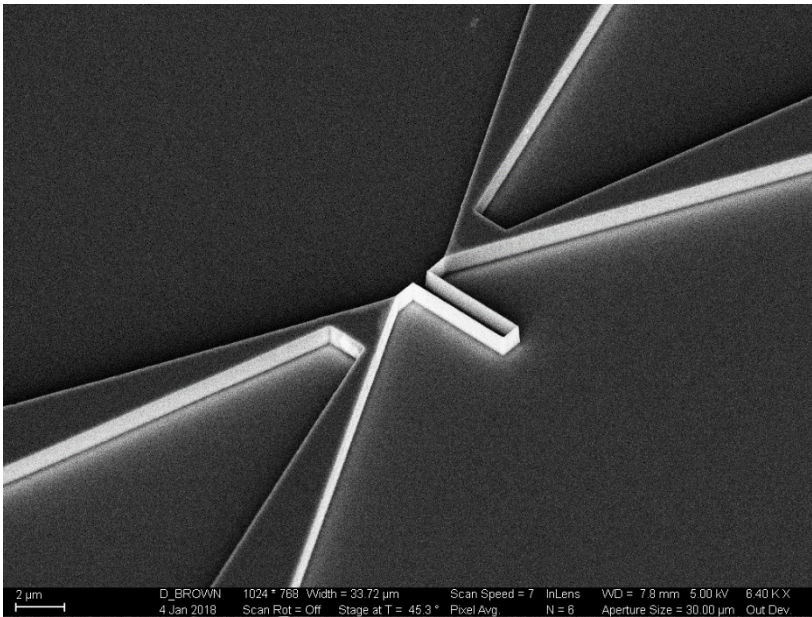
7/13/2020

ICP Etch Process

- etch tool = Plasma-Therm ICP
- recipe
 - pressure = 5 mTorr
 - 50 sccm Cl₂
 - coil 125 W
 - plate 75 W
 - (typical DC Bias = 450V)
- etch rates
 - silicon etch rate = 87 nm/min
 - HSQ etch rate = 13 nm/min
 - selectivity = 6.7

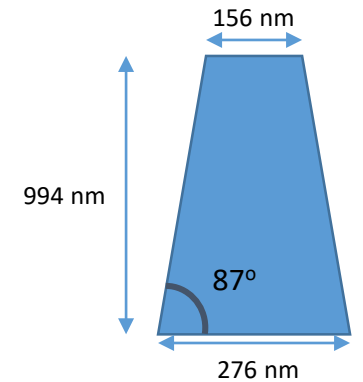
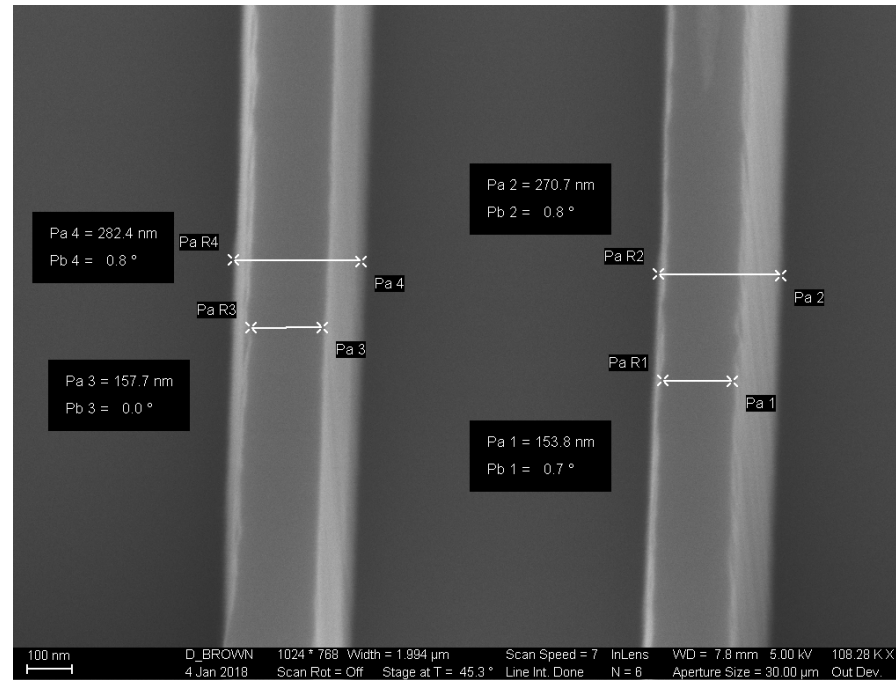
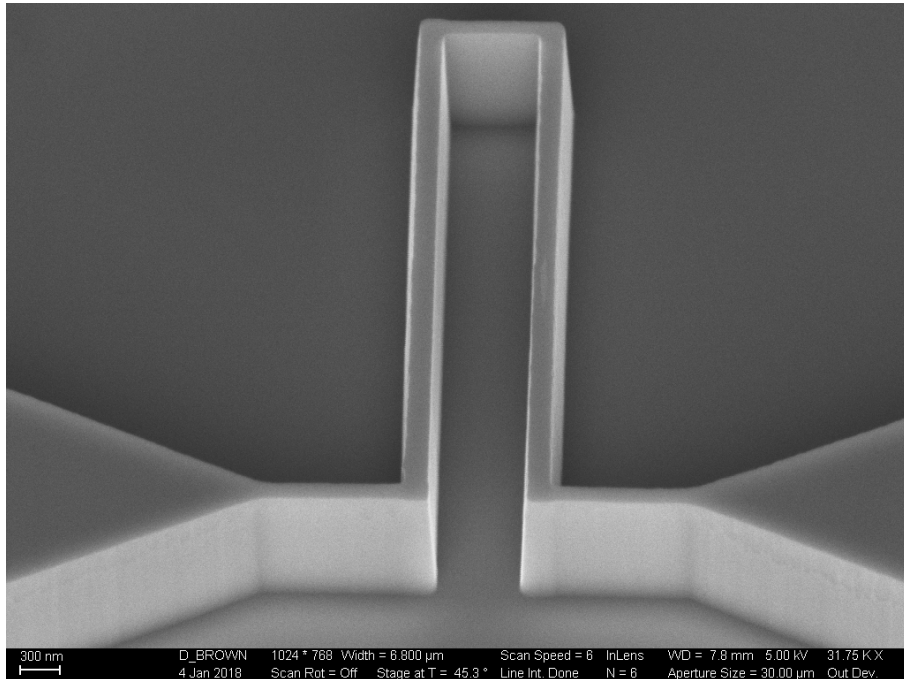


SEM results



- serpentine resistor pattern with four electrode connections
- minimum linewidth 27 – 52 nm
- etch depth = 994 nm

SEM Results



- serpentine resistor pattern with four electrode connections
- minimum linewidth 154 – 158 nm, etch depth = 994 nm
- sidewall angle = 87°