“nano-Bosch” etching silicon with PMMA resist mask

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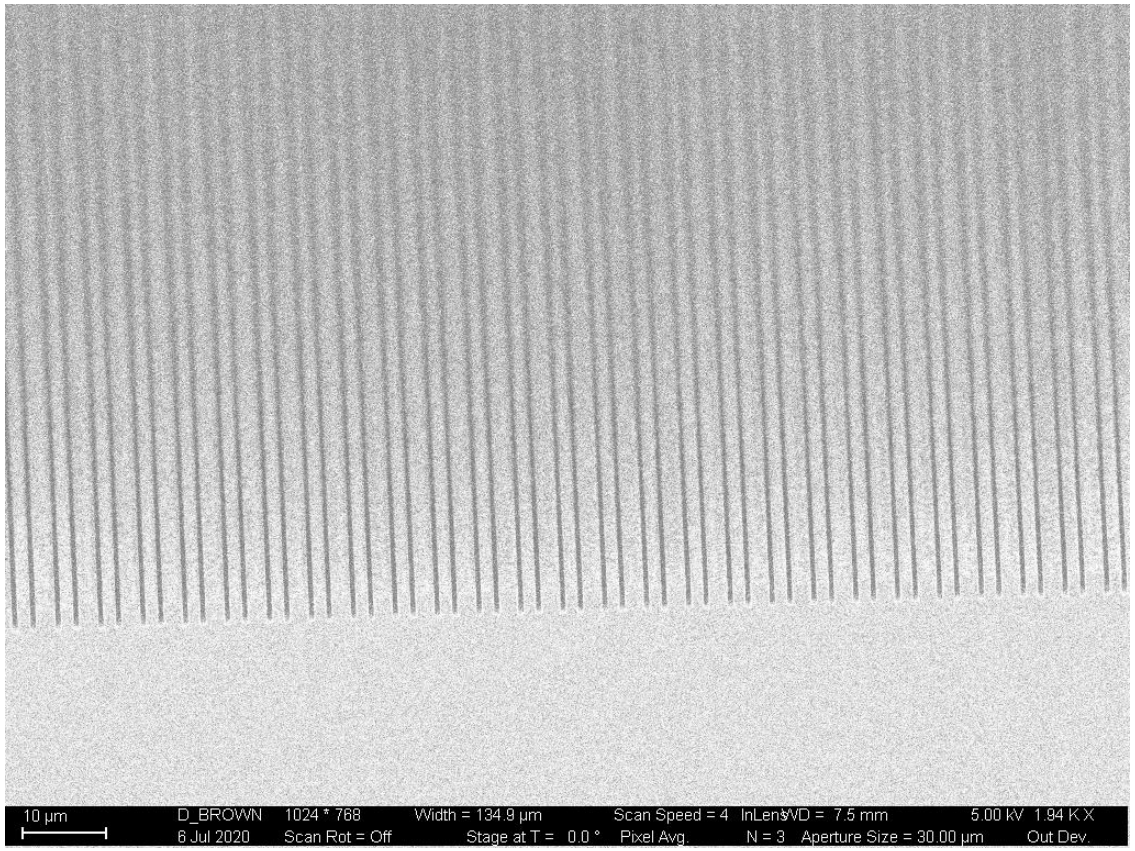
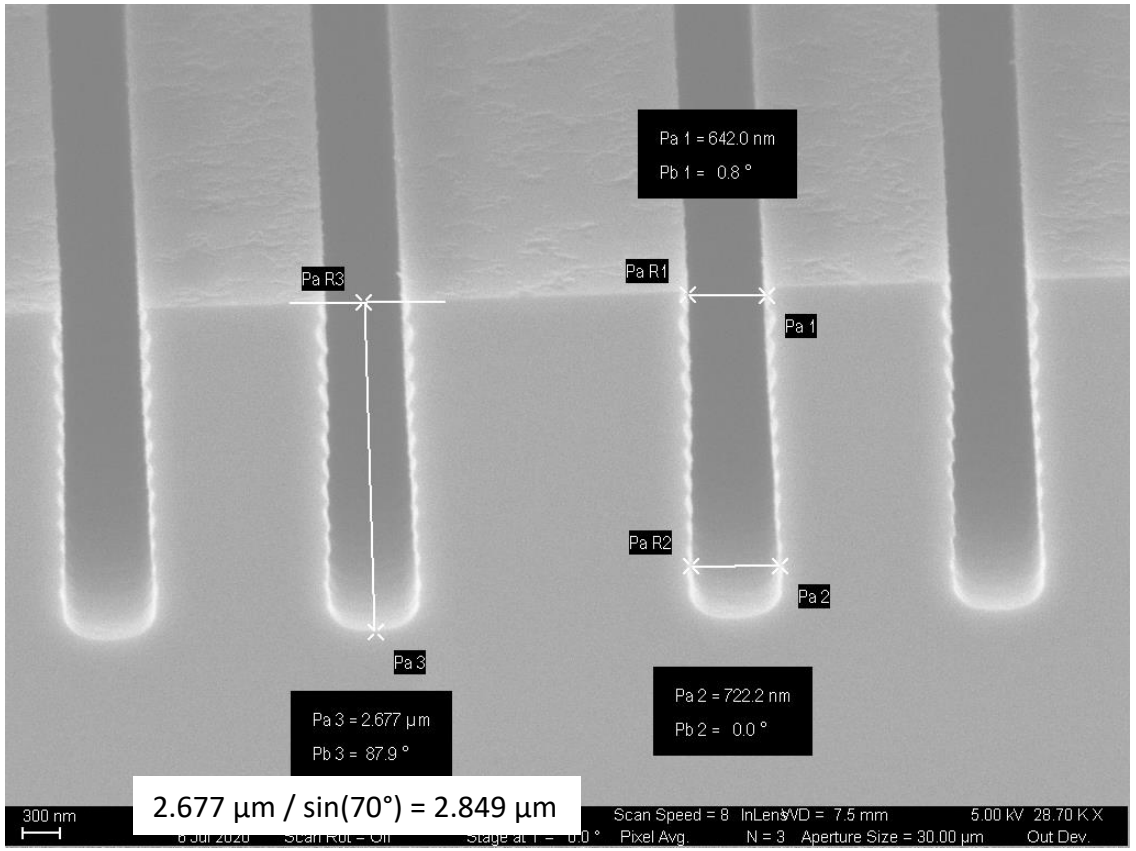
“nano-Bosch” Etch process

- etch tool = STS ICP
- recipe
  - APC mode = manual, APC setting = 71.5%, effective pressure = 10 mTorr
  - passivate step
    - time = 9 sec, C4F8 = 100 sccm, coil = 600 W, plate = OFF, freq = 13.56 MHz
  - etch step
    - time = 6 sec, SF6 = 60 sccm, O2 = 15 sccm, coil = 600 W, plate = 11 W, freq = 13.56 MHz
  - helium back side cooling = active
- etch rates
  - Si = 212 - 249 nm / cycle
  - PMMA = 6 - 9 nm / cycle
  - selectivity = 27 – 33

SEM results

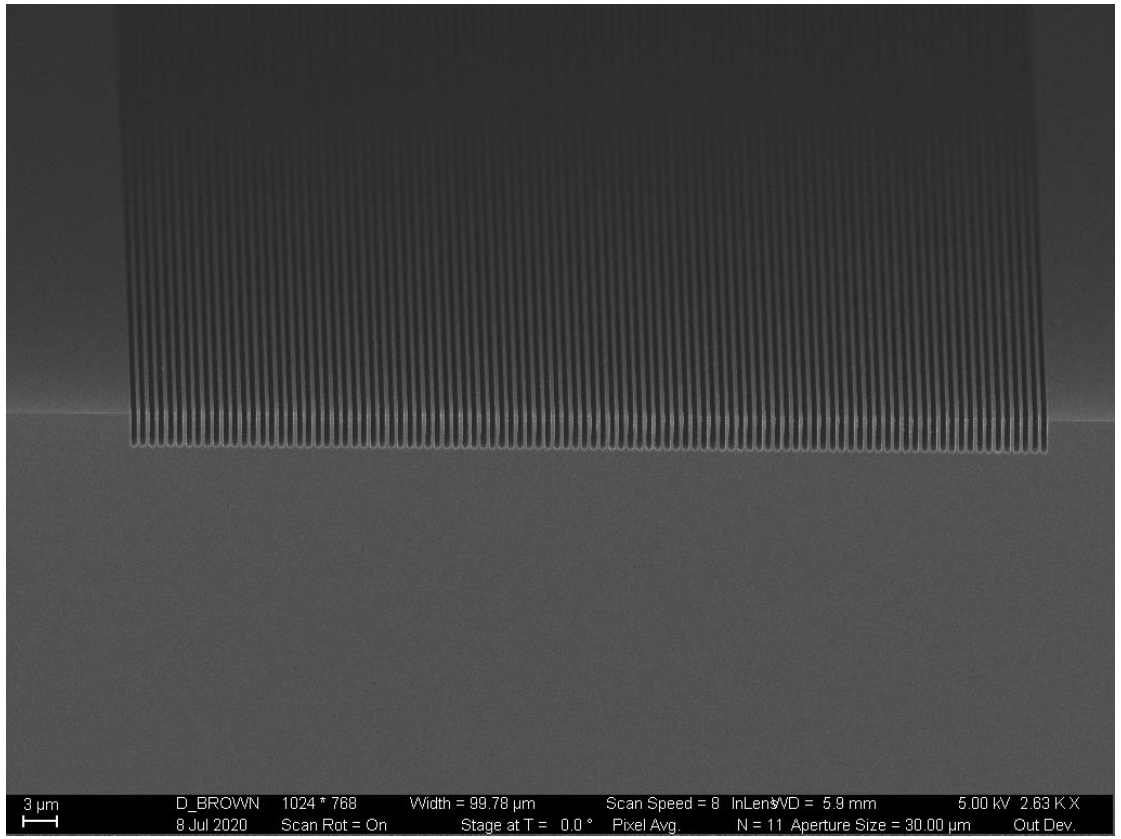


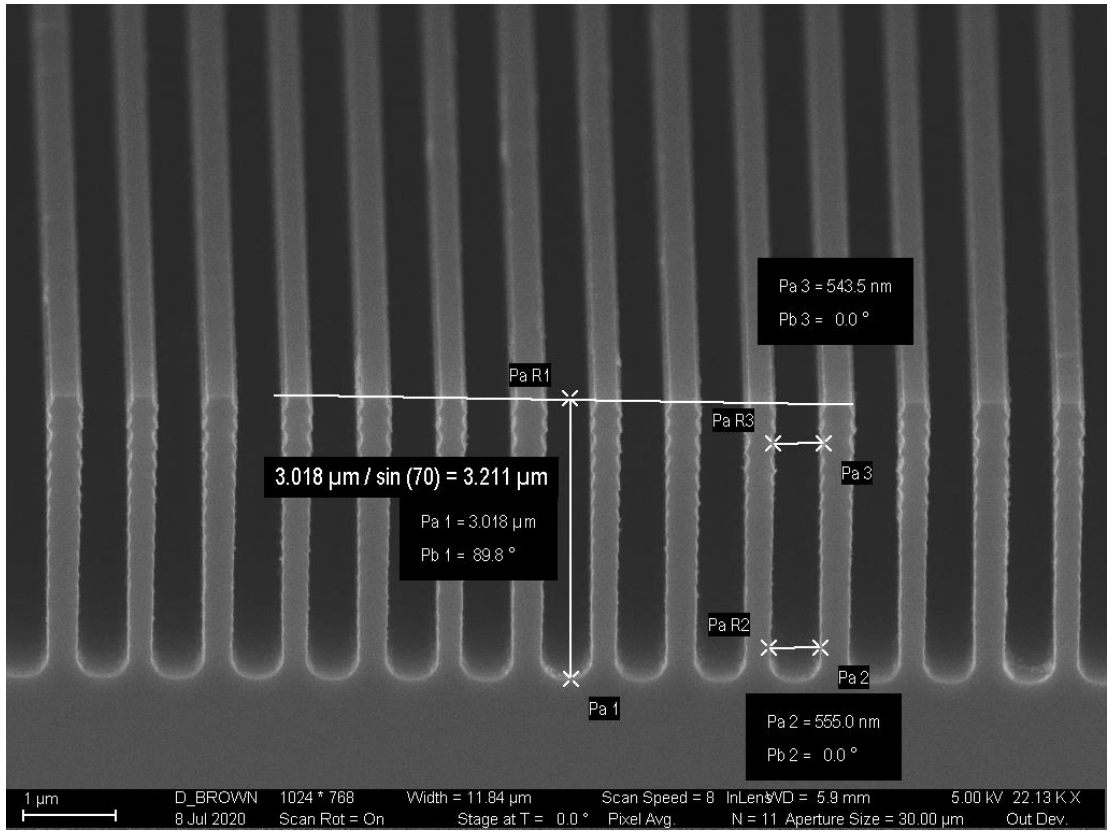


2.677 µm / sin(70°) = 2.849 µm

- etched silicon, post resist removal
- pattern = 642 nm lines / 2.1 µm pitch / 5.0 µm pitch
- snap cleave cross section
- SEM image sample at 70° tilt
- etch cycles = 14, etch depth = 2.849 µm

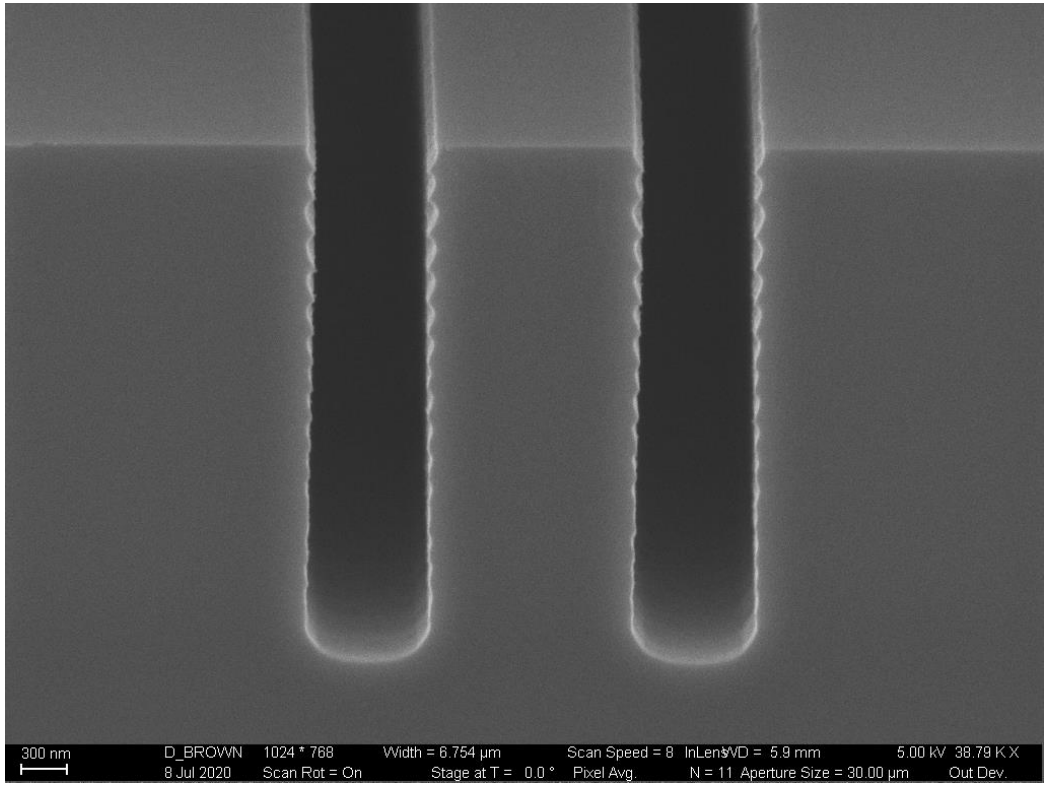
SEM results



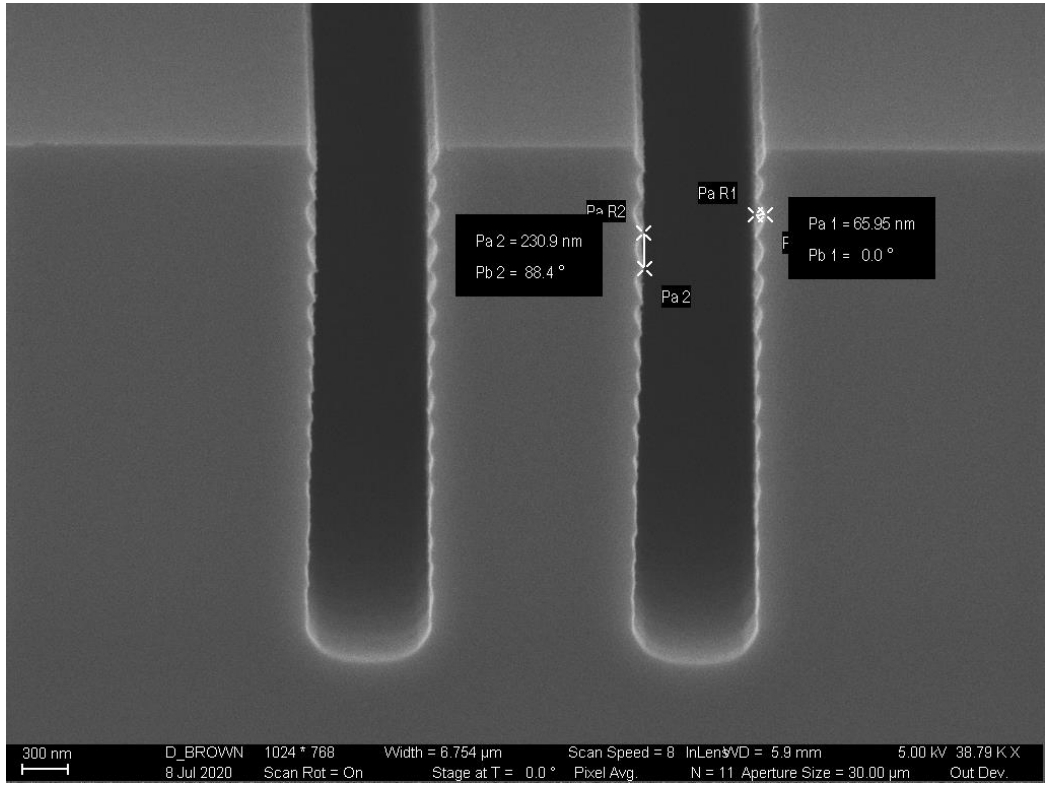


- etched silicon, post resist removal
- pattern = 543 nm lines / 800 nm pitch
- snap cleave cross section
- SEM image sample at 70° tilt
- etch cycles = 18, etch depth = 3.211 µm

SEM results

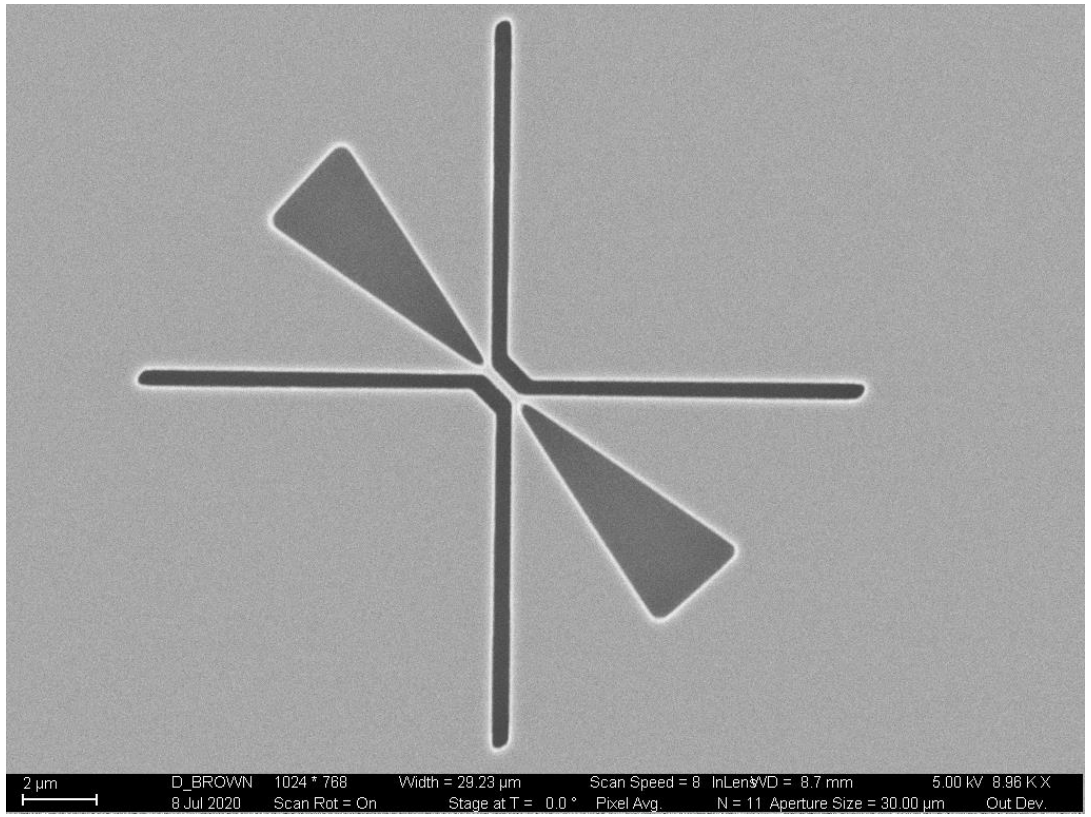


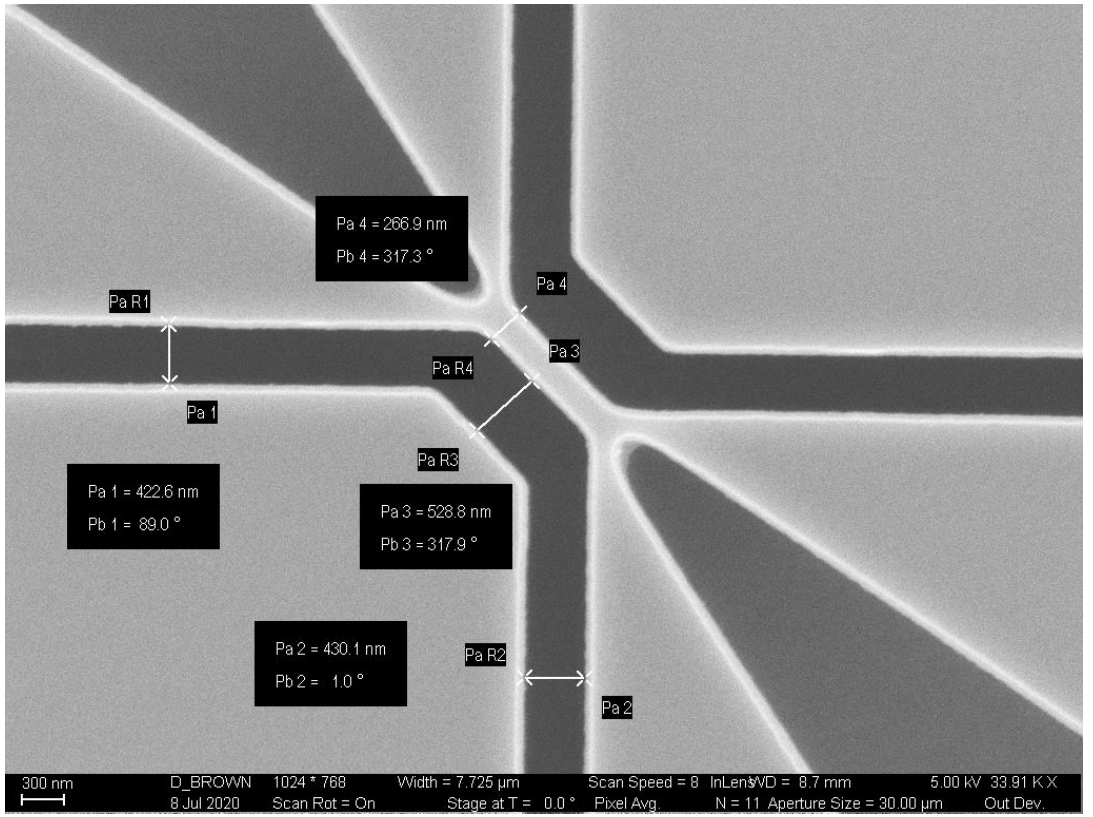
- etched silicon, post resist removal
- pattern = 543 nm lines / 800 nm pitch
- snap cleave cross section
- SEM image sample at 70° tilt
- etch cycles = 18, etch depth = 3.211 µm



- scalloping more towards top, smoother at bottom
- vertical scallop length = ~231 nm (varies)
- lateral scallop sidewall roughness = ~66 nm (varies)

SEM results





- etched silicon, post resist removal
- device pattern, top down image
- minimum etch gap/trench = 423 nm
- minimum silicon fin width = 267 nm